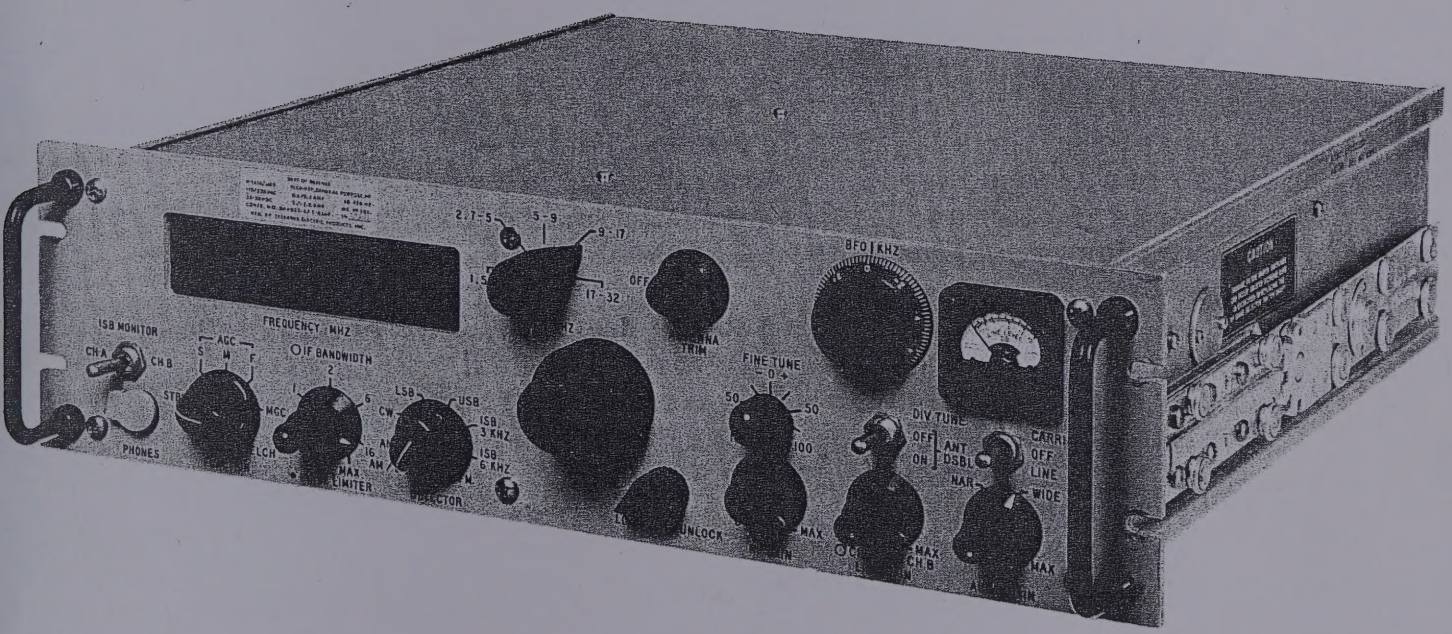
TEMO-459-010A

R-1414/URR
HF GENERAL PURPOSE
RADIO RECEIVER

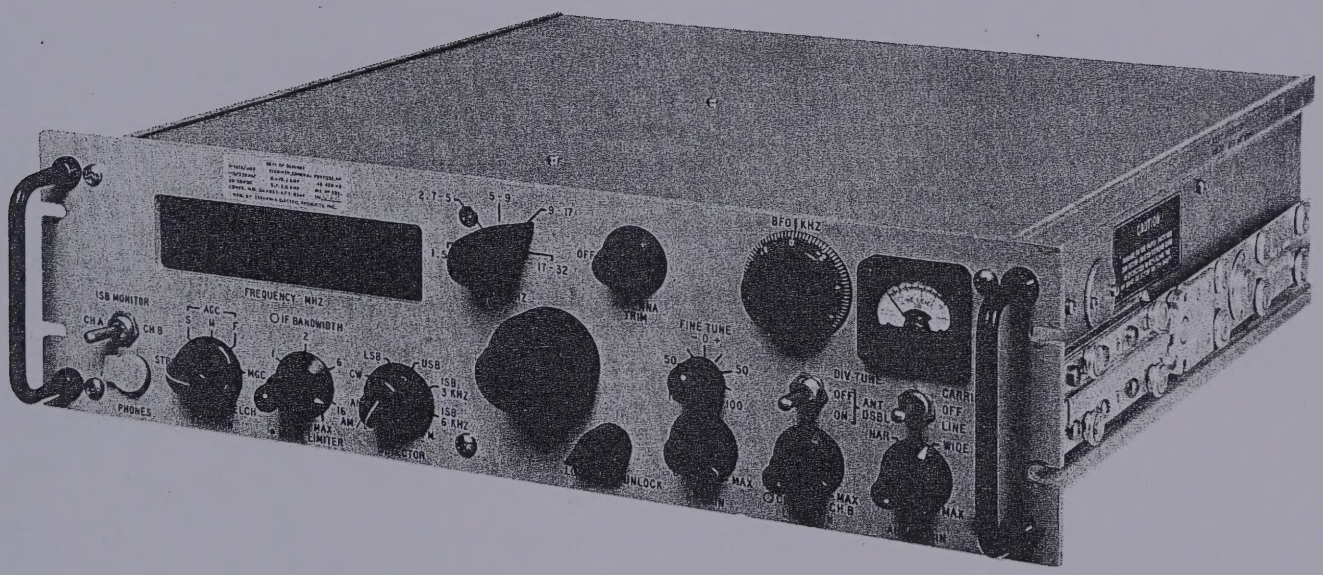


TECHNICAL MANUAL

OCTOBER 1970

TEMO-459-010A

R-1414/URR
HF GENERAL PURPOSE
RADIO RECEIVER



TECHNICAL MANUAL

OCTOBER 1970

TEMO-459-010A

R1414/URR
RECEIVER, RADIO,
GENERAL PURPOSE, HF

SYLVANIA ELECTRONIC SYSTEMS-WESTERN DIVISION
P. O. Box 188
Mountain View, California 94040

Contract No. DAAB03-67-C-0369

TECHNICAL MANUAL

OCTOBER 1970

FOR OFFICIAL USE ONLY

INTRODUCTION

This instruction manual contains information pertinent to installing, operating, maintaining and troubleshooting the R-1414/URR HF General Purpose Radio Receiver. Chapter 1 contains general information about the equipment. Chapter 2 provides site selection and installation procedures. Chapter 3 furnishes functional descriptions of operating controls and indicators and complete operating instructions. Chapter 4 contains a block diagram description, and functional descriptions of major receiver subassemblies; Chapter 5 provides preventive maintenance procedures which are designed to maintain the receiver in operating status with a minimum of down time. Chapter 6 provides instructions for locating and correcting malfunctions in the receiver, repairing defective parts, and provides complete alignment and adjustment procedures. Chapter 7 contains an illustrated parts breakdown for the receiver. Appendix A contains all the detailed schematic and interconnection diagrams for the receiver and its subassemblies. Appendix B contains wire lists of the overall receiver, counter A9, and the ac and dc input power supplies.

This instruction manual has been prepared to serve the needs and requirements of a graduate of military service school course in basic electronics. Before using the maintenance procedures in Chapters 5 and 6, the principles of operation (Chapter 4) should be read and understood.

TABLE OF CONTENTS

CHAPTER 1

DESCRIPTION OF EQUIPMENT

Paragraph		Page
1 - 1	GENERAL	1 - 1
1 - 2	CLASSIFICATION	1 - 1
1 - 3	PURPOSE AND DESCRIPTION	1 - 1
1 - 4	TECHNICAL CHARACTERISTICS	1 - 6
1 - 5	EQUIPMENT SUPPLIED	1 - 6
1 - 6	EQUIPMENT REQUIRED BUT NOT SUPPLIED	1 - 6
1 - 7	OPTIONAL EQUIPMENT	1 - 6

CHAPTER 2

INSTALLATION

2 - 1	GENERAL	2 - 1
2 - 2	SITE SELECTION	2 - 1
2 - 2a	Power Requirements	2 - 1
2 - 2b	Antenna Requirements	2 - 1
2 - 3	INSTALLATION PROCEDURES	2 - 1
2 - 3a	Placement and Mounting	2 - 1
2 - 3b	Power Cables	2 - 2
2 - 3c	Rear-Panel Connections and Controls	2 - 2
2 - 3d	Single-receiver Operation	2 - 2
2 - 3e	Diversity Operation	2 - 2
2 - 4	INITIAL CHECKOUT AND ADJUSTMENTS	2 - 2

CHAPTER 3

OPERATING INSTRUCTIONS

3 - 1	GENERAL	3 - 1
3 - 2	OPERATING CONTROLS, INDICATORS, AND CONNECTORS	3 - 1
3 - 3	STARTING PROCEDURE	3 - 6
3 - 4	NORMAL OPERATING PROCEDURES	3 - 7
3 - 4a	AM Signal Reception	3 - 7
3 - 4b	CW Signal Reception	3 - 7
3 - 4c	SSB Signal Reception	3 - 8
3 - 4d	ISB Signal Reception	3 - 9
3 - 4e	FM Signal Reception	3 - 9
3 - 4f	Frequency-Shift Keying Signal Reception	3 - 10
3 - 4g	Diversity Operation	3 - 11
3 - 4h	Antijamming Instructions	3 - 11
3 - 5	STOPPING PROCEDURE	3 - 12

TABLE OF CONTENTS (Continued)

CHAPTER 4

PRINCIPLES OF OPERATION

Paragraph		Page
4 - 1	GENERAL	4 - 1
4 - 2	OVERALL BLOCK DIAGRAM DESCRIPTION	4 - 1
4 - 2a	RF Section	4 - 1
4 - 2b	Counter and AFC	4 - 2
4 - 2c	AF/IF Section	4 - 12
4 - 3	POWER DISTRIBUTION	4 - 17
4 - 4	FUNCTIONAL OPERATION OF ELECTRONIC CIRCUITS	4 - 17
4 - 4a	Electrical RF Connector Assembly A16	4 - 17
4 - 4b	Antenna Tuner A1	4 - 17
4 - 4c	RF Tuners A2, A4, and A5	4 - 18
4 - 4d	Tuner Subassembly A21	4 - 18
4 - 4e	RF Amplifier A3	4 - 21
4 - 4f	First Mixer A6	4 - 22
4 - 4g	First Local Oscillator A7A1	4 - 24
4 - 4h	AFC and Electronic Digital Readout Counter, A8 and A9	4 - 26
4 - 4i	First IF Amplifier A10	4 - 49
4 - 4j	Second Mixer A11	4 - 51
4 - 4k	Second Local Oscillator A18	4 - 55
4 - 4l	Second IF Amplifier	4 - 55
4 - 4m	Detector A13	4 - 57
4 - 4n	Independent Sideband (ISB) A14	4 - 61
4 - 4o	AF Amplifier A15	4 - 64
4 - 4p	Beat Frequency Oscillator A22	4 - 66
4 - 4q	AC Input Power Supply PS1	4 - 67
4 - 4r	DC Input Power Supply PS2	4 - 73
4 - 4s	Filters	4 - 74

CHAPTER 5

PREVENTIVE MAINTENANCE

5 - 1	GENERAL	5 - 1
5 - 2	PREVENTIVE MAINTENANCE EQUIPMENT	5 - 1
5 - 3	SCHEDULE FOR PERIODIC MAINTENANCE	5 - 2
5 - 4	PURPOSE OF PREVENTIVE MAINTENANCE	5 - 3
5 - 4a	Inspections	5 - 3
5 - 4b	Cleaning	5 - 3
5 - 5	VISUAL INSPECTION	5 - 3
5 - 6	CLEANING	5 - 3
5 - 7	LUBRICATION	5 - 4
5 - 7a	Tuner Subassembly A21	5 - 4
5 - 7b	Band Change Gear Box MP1	5 - 4
5 - 7c	Rotary Switches	5 - 7
5 - 8	PERFORMANCE CHECK	5 - 7

TABLE OF CONTENTS (Continued)

CHAPTER 6

CORRECTIVE MAINTENANCE

Paragraph		Page
6 - 1	GENERAL	6 - 1
6 - 2	CORRECTIVE MAINTENANCE TEST EQUIPMENT	6 - 1
6 - 3	GENERAL TESTING INFORMATION	6 - 3
6 - 3a	Test Points	6 - 3
6 - 3b	Voltage Measurements	6 - 3
6 - 3c	Resistance Measurements	6 - 3
6 - 3d	Intermittant Troubles	6 - 4
6 - 3e	Transistor Testing	6 - 4
6 - 4	PERFORMANCE TESTING	6 - 10
6 - 4a	Nominal Test Point Voltages and Waveforms	6 - 10
6 - 4b	Performance Tests	6 - 16
6 - 5	ALIGNMENT AND ADJUSTMENT	6 - 51
6 - 5a	First Local Oscillator Alignment	6 - 52
6 - 5b	RF Tuner Alignment Using HF Signal Generator	6 - 53
6 - 5c	RF Tuner Alignment Using Sweep Generator	6 - 55
6 - 5d	Automatic Gain Control	6 - 57
6 - 5e	Squelch	6 - 59
6 - 5f	Second Local Oscillator A18	6 - 60
6 - 5g	AFC A8	6 - 60
6 - 5h	RF Oscillator A9Y1	6 - 60
6 - 5i	Second IF Amplifier A12	6 - 60
6 - 5j	ISB A14	6 - 61
6 - 5k	BFO KHZ Control Centering and Accuracy (frequency counter method)	6 - 62
6 - 5l	BFO Knob Center and Accuracy (Zero beat method)	6 - 62
6 - 5m	Power Supply Adjustment	6 - 63
6 - 6	GENERAL TROUBLESHOOTING INFORMATION	6 - 64
6 - 7	TROUBLESHOOTING	6 - 64
6 - 8	REMOVAL AND REPLACEMENT OF SUBASSEMBLIES	6 - 69
6 - 8a	Printed Circuit Boards	6 - 69
6 - 8b	Front Panel	6 - 71
6 - 8c	BFO KHZ Capacitor C2	6 - 72
6 - 8d	ANTENNA TRIM Capacitor C1	6 - 72
6 - 8e	Tuner Subassembly A21	6 - 72
6 - 8f	Counter A9	6 - 73
6 - 8g	Gear Assembly MP1	6 - 74
6 - 8h	Electrical RF Section Counter Assembly A16	6 - 74
6 - 8i	Beat Frequency Oscillator (BFO) A22	6 - 74
6 - 8j	Second Local Oscillator A18	6 - 75
6 - 8k	Filters FL1 through FL3	6 - 75
6 - 8l	Filters FL4 through FL10	6 - 75
6 - 8m	Filter FL19	6 - 76
6 - 8n	Lamp A21DS1	6 - 76
6 - 8o	Power Supply PS1 or PS2	6 - 76

TABLE OF CONTENTS (Continued)

Paragraph		Page
6 - 9	GENERAL REPLACEMENT TECHNIQUES	6 - 78
6 - 10	PRINTED CIRCUIT CARD MAINTENANCE	6 - 78
6 - 10a	Test Equipment and Special Tools Required	6 - 78
6 - 10b	Printed Circuit Card Part Removal	6 - 80
6 - 10c	Printed Circuit Card Part Replacement	6 - 80
6 - 10d	Printed Wiring Repair	6 - 81
	CHAPTER 7	
	ILLUSTRATED PARTS BREAKDOWN	
7 - 1	INTRODUCTION	7 - 1
7 - 2	GROUP ASSEMBLY PARTS LIST	7 - 9
7 - 3	NUMERICAL INDEX	7 - 117
7 - 4	REFERENCE DESIGNATOR INDEX	7 - 139
7 - 5	STOCK NUMBER INDEX	7 - 181
	APPENDIX A	
	DIAGRAMS	
A - 1	GENERAL	A - 1
A - 2	SYMBOLS	A - 1
A - 3	INTEGRATED CIRCUITS	A - 1
A - 4	TEST DATA	A - 1
A - 5	NONSTANDARD ABBREVIATIONS	A - 1
A - 6	TRANSISTOR AND INTEGRATED CIRCUIT BASE TERMINAL DIAGRAMS	A - 2
	APPENDIX B	
	WIRE LISTS	
B - 1	GENERAL	B - 1
B - 2	RADIO RECEIVER R-1414/URR, WIRE LIST	B - 1
B - 3	COUNTER A9, WIRE LIST	B - 1
B - 4	AC INPUT POWER SUPPLY PS1, WIRE LIST	B - 1
B - 5	DC INPUT POWER SUPPLY PS2, WIRE LIST	B - 1

LIST OF ILLUSTRATIONS

Fig. No.	Description	Page
1 - 1	R-1414/URR, HF General Purpose Radio Receiver	1 - 0
1 - 2	Receiver Top View Identifying Major Components	1 - 3
1 - 3	Receiver Bottom View Identifying Major Components	1 - 4
2 - 1	Receiver Interface Drawing	2 - 3
2 - 2	Receiver with Slide Drawer Extension	2 - 5
2 - 3	Power Cable Schematics	2 - 6
2 - 4	Receiver Rear View, Identifying Controls and Indicators	2 - 7
2 - 5	Single Receiver Operation, Interconnection Diagram	2 - 11
2 - 6	Diversity Receiver Operation, Interconnection Diagram	2 - 13
3 - 1	Receiver Front Panel, Operating Controls, and Indicators	3 - 1
4 - 1	R-1414/URR HF General Purpose Radio Receiver Block Diagram	4 - 3
4 - 2	Double-Tuned Filter	4 - 11
4 - 3	AGC Loop, Simplified Block Diagram	4 - 14
4 - 4	Power Distribution Diagram	4 - 19
4 - 5	RF Amplifier A3, Block Diagram	4 - 22
4 - 6	First Mixer A6, Block Diagram	4 - 23
4 - 7	First Mixer A6, Simplified Schematic Diagram	4 - 24
4 - 8	First Local Oscillator A7A1	4 - 25
4 - 9	AFC Loop and Counter, Block Diagram	4 - 27
4 - 10	Counter Timing Diagram	4 - 29
4 - 11	Gate Generator A9A2, Block Diagram	4 - 31
4 - 12	Divider A9A3, Block Diagram	4 - 32
4 - 13	Display A9A1, Block Diagram	4 - 33
4 - 14	Four 2-Input NAND/NOR Gate (ONO53338-1), Logic Diagram	4 - 35
4 - 15	Two 5-Input NAND/NOR Gate (ONO53339-1), Logic Diagram	4 - 36
4 - 16	Three 3-Input NAND/NOR Gate (ONO53340-1), Logic Diagram	4 - 37
4 - 17	Four 2-Input NAND/NOR Gate (ONO53341-1), Logic Diagram	4 - 38
4 - 18	Dual J-K Flip-Flop (ONO53335-1), Logic Diagram	4 - 39
4 - 19	AND Input J-K Flip-Flop (ONO53333-1), Logic Diagram	4 - 41
4 - 20	Decade Counter (ONO53342-1), Logic Diagram	4 - 43
4 - 21	BCD-to-Decimal Decoder Driver (ONO53337-1), Logic Diagram	4 - 44
4 - 22	2-Bit Binary Full Adders (ONO53336-1), Logic Diagram	4 - 46
4 - 23	Automatic Frequency Control (AFC) A8, Block Diagram	4 - 48
4 - 24	AFC Loop Probability of Correction versus Frequency Error	4 - 49
4 - 25	First IF Amplifier A10, Block Diagram	4 - 50
4 - 26	Current-Controlled Attenuator	4 - 51
4 - 27	Second Mixer A11, Block Diagram	4 - 52
4 - 28	Second IF Amplifier A12, Block Diagram	4 - 56
4 - 29	Detector A13, Block Diagram	4 - 59
4 - 30	Independent Sideband (ISB) A14, Block Diagram	4 - 62
4 - 31	FM Detector Characteristic	4 - 63
4 - 32	AF Amplifier A15, Block Diagram	4 - 65
4 - 33	BFO Block Diagram	4 - 67
4 - 34	Power Supply PS1, Block Diagram	4 - 69
4 - 35	Bendback Short Circuit Protection Characteristics	4 - 71
4 - 36	Power Supply PS2, Block Diagram	4 - 75

LIST OF ILLUSTRATIONS (Continued)

Fig. No.	Description	Page
5 - 1	Tuner Subassembly Gear Box	5 - 5
5 - 2	Band Change Gear Box MP1	5 - 7
5 - 3	Noise Figure, Test Setup Diagram	5 - 14
5 - 4	Sensitivity Check, Test Setup Diagram	5 - 15
5 - 5	Overall Gain, Test Setup Diagram	5 - 15
6 - 1	Receiver Top View, RFI Covers Installed	6 - 11
6 - 2	RF Section, Identification of Controls and Test Points	6 - 12
6 - 3	Counter Section, Identification of Test Points	6 - 13
6 - 4	AF/IF Section, Identification of Controls and Test Points	6 - 14
6 - 5	Power Supplies, PS1 and PS2, Identification of Test Points	6 - 15
6 - 6	Basic Test Setup Diagram	6 - 16
6 - 7	Noise Figure Test Setup Diagram	6 - 29
6 - 8	Sensitivity Check, Test Setup Diagram	6 - 31
6 - 9	Overall Gain, Test Setup Diagram	6 - 35
6 - 10	Carrier Meter and Line Level Meter, Test Setup Diagram	6 - 41
6 - 11	Noise Suppression, Test Setup No. 1	6 - 42
6 - 12	Noise Suppression, Test Setup No. 2	6 - 44
6 - 13	Automatic Gain Control, Test Setup Diagram	6 - 46
6 - 14	BFO Range and Dial Marking Accuracy (Counter Method), Test Setup Diagram	6 - 47
6 - 15	BFO Range and Dial Marking Accuracy (Zero Beat Method), Test Setup Diagram	6 - 49
6 - 16	Receiver Bottom View Identifying Test Points and Controls	6 - 52
6 - 17	RF Tuner Alignment (Sweep Generator), Test Setup Diagram	6 - 57
6 - 18	AGC Alignment, Test Setup Diagram	6 - 58
6 - 19	Receiver Troubleshooting Chart	6 - 65
6 - 20	AC Input Power Supply, Troubleshooting Chart	6 - 67
6 - 21	DC Input Power Supply, Troubleshooting Chart	6 - 68
6 - 22	Printed Circuit Board Puller	6 - 70
7 - 1	Radio Receiver (R-1414/URR) (ONO53500-2)	7 - 9
7 - 2	BFO A22, Circuit Card Assembly (ONO53680-1)	7 - 28
7 - 3	First Local Oscillator A7 (ONO53576-1)	7 - 30
7 - 4	First Mixer A6, Circuit Card Assembly (ONO53564-1)	7 - 37
7 - 5	RF Tuner A2, 4, 5, Circuit Card Assembly (ONO53601-1)	7 - 40
7 - 6	Antenna Tuner A1, Circuit Card Assembly (ONO53556-2)	7 - 42
7 - 7	AFC A8, Circuit Card Assembly (ONO53568-2)	7 - 45
7 - 8	RF Amplifier A3, Circuit Card Assembly (ONO53560-2)	7 - 49
7 - 9	Electronic Digital Readout Counter, A9 (ONO53577-2)	7 - 52
7 - 10	Gate Generator A9A2, Circuit Card Assembly (ONO53539-1)	7 - 55
7 - 11	Driver A9A3, Circuit Card Assembly (ONO53543-1)	7 - 58
7 - 12	Display A9A1, Circuit Card Assembly (ONO53535-2)	7 - 61
7 - 13	ISB A14, Circuit Card Assembly (ONO53523-2)	7 - 64
7 - 14	Detector A13, Circuit Card Assembly (ONO53519-2)	7 - 68
7 - 15	Second IF Amplifier A12, Circuit Card Assembly (ONO53593-2)	7 - 72
7 - 16	Second Mixer A11, Circuit Card Assembly (ONO53515-2)	7 - 77
7 - 17	First IF Amplifier A10, Circuit Card Assembly (ONO53511-1)	7 - 82
7 - 18	AF Amplifier A15, Circuit Card Assembly (ONO53527-2)	7 - 86
7 - 19	Adapter Test A23 (ONO53674-1)	7 - 92
7 - 20	RF Connector A16, Circuit Card Assembly (ONO53551-2)	7 - 94

LIST OF ILLUSTRATIONS (Continued)

Fig. No.	Description	Page
7 - 22	Power Supply PS1 ONO53349-2 (AC), PS2 ONO53349-3 (DC) (Optional)	7 - 96
7 - 23	Voltage Regulator PS1A1 ONO53703-2 (AC), PS2A1 ONO53703-3 (DC) (Optional)	7 - 98
7 - 24	Voltage Regulator, Circuit Card Assembly PS1A2 ONO53707-2 (AC), PS2A2 ONO53707-3 (DC) (Optional)	7 - 105
7 - 25	Converter DC-AC PS2A3, Circuit Card Assembly, ONO53716-1 (DC) (Optional)	7 - 109
A - 1	Transistor and Integrated Circuit Base Terminal Diagrams	A - 3
A - 2	Reference Designator Breakdown	A - 5
A - 3	HF General Purpose Receiver Radio Receiver R-1414/URR (ONO53500-2), Interconnection Diagram	A - 7
A - 4	Electrical RF Connector Assembly A16 (ONO53551-2), Schematic Diagram	A - 15
A - 5	Antenna Tuner A1 (ONO53556-2), Schematic Diagram	A - 19
A - 6	RF Tuner A2, A4, and A5 (ONO53601), Schematic Diagram	A - 23
A - 7	Tuner Subassembly A21 (ONO53644-2), Schematic Diagram	A - 25
A - 8	RF Amplifier A3 (ONO53560-2), Schematic Diagram	A - 27
A - 9	First Mixer A6 (ONO53564-1), Schematic Diagram	A - 29
A - 10	First Local Oscillator A7A1 (ONO53576-1), Schematic Diagram	A - 31
A - 11	Electronic Digital Readout Counter A9 (ONO53577-2), Interconnection Diagram	A - 35
A - 12	Display A9A1 (ONO53535-2), Schematic Diagram	A - 37
A - 13	Gate Generator A9A2 (ONO53539-1), Schematic Diagram	A - 41
A - 14	Divider A9A3 (ONO53547-1), Schematic Diagram	A - 45
A - 15	Automatic Frequency Control (AFC) (ONO53568-2), Schematic Diagram	A - 49
A - 16	First IF Amplifier A10 (ONO53511-1), Schematic Diagram	A - 51
A - 17	Second Mixer A11 (ONO53515-2), Schematic Diagram	A - 55
A - 18	Second IF Amplifier A12 (ONO53593-2), Schematic Diagram	A - 59
A - 19	Detector A13 (ONO53519-1), Schematic Diagram	A - 63
A - 20	Independent Sideband (ISB) (ONO53523-2), Schematic Diagram	A - 67
A - 21	AF Amplifier A15 (ONO53527-2), Schematic Diagram	A - 71
A - 22	Beat Frequency Oscillator A22 (ONO53680-1), Schematic Diagram	A - 75

LIST OF ILLUSTRATIONS (Continued)

Fig. No.	Description	Page
A - 23	AC Input Power Supply PS1 (ONO53349-2), Schematic Diagram	A - 77
A - 24	+25 Volt and -8 Volt Regulator (PS1A1 and Optional PS2A1), Schematic Diagram	A - 79
A - 25	+230 Volt and +5 Volt Regulator (PS1A1 and Optional PS2A2), Schematic Diagram	A - 81
A - 26	Optional DC Input Power Supply PS2 (ONO53349-3), Schematic Diagram	A - 83
A - 27	Optional DC to AC Converter PS2A3, Schematic Diagram	A - 85
A - 28	HF General Purpose Radio Receiver R-1414/URR (ONO53500-2), Schematic Diagram	A - 87

LIST OF TABLES

Number	Description	Page
1 - 1	Designation of Received Emissions	1 - 2
1 - 2	Major Subassemblies	1 - 5
1 - 3	Technical Characteristics	1 - 6
1 - 4	Equipment Supplied	1 - 9
1 - 5	Equipment Required But Not Supplied	1 - 9
1 - 6	Optional Equipment	1 - 10
2 - 1	Rear Panel Controls and Connections	2 - 8
3 - 1	Operating Controls and Indicators	3 - 2
4 - 1	Input, LO, and First IF Frequencies	4 - 11
4 - 2	FUNCTION Switch S1	4 - 14
4 - 3	DETECTOR Switch S3	4 - 16
4 - 4	Integrated Circuit Cross Reference List	4 - 34
4 - 5	First Part of AGC Decay Time	4 - 53
4 - 6	Second Part of AGC Decay Time	4 - 54
4 - 7	IF and LO Frequencies	4 - 55
4 - 8	AC Power Supply Specifications	4 - 67
4 - 9	Filter Specifications	4 - 74
5 - 1	Preventive Maintenance Test Equipment	5 - 1
5 - 2	Recommended Maintenance Schedule	5 - 2
5 - 3	Performance Check	5 - 8
6 - 1	Corrective Maintenance Test Equipment	6 - 1
6 - 2	Transistor Bias Voltages	6 - 4
6 - 3	Normal Test Point Outputs	6 - 17
6 - 4	Noise Figure (Noise Generator Method), Performance Test	6 - 28
6 - 5	Sensitivity Check (Alternate for Noise Figure), Performance Test	6 - 30

LIST OF TABLES (Continued)

Number	Description	Page
6 - 6	Overall Gain, Audio Power, IF Output, Performance Tests	6 - 32
6 - 7	IF Gain, Performance Tests	6 - 35
6 - 8	Overall Selectivity, Performance Test	6 - 36
6 - 9	Antenna Grounding Relay Attenuation, Performance Test	6 - 38
6 - 10	Carrier Meter and Line Level Meter, Performance Test	6 - 40
6 - 11	Noise Suppression (Pulse Generator Method), Performance Test	6 - 41
6 - 12	Noise Suppression (Noise Source Method), Performance Test	6 - 43
6 - 13	Automatic Gain Control, Performance Test	6 - 44
6 - 14	BFO Range and Dial Marking Accuracy (Counter Method), Performance Test	6 - 46
6 - 15	BFO Range and Dial Marking Accuracy (Zero-Beat Method), Performance Test	6 - 48
6 - 16	Dial Lock, Performance Test	6 - 50
6 - 17	Motion Detector, Performance Test	6 - 50
6 - 18	Alignment and Adjustment Listing	6 - 51
6 - 19	Local Oscillator Controls	6 - 53
6 - 20	RF Tuner Controls	6 - 54
6 - 21	RF Tuner Controls and IF Bandwidth	6 - 56
6 - 22	Tools and Materials Required for Printed Circuit Card Repair	6 - 78
6 - 23	Tools and Materials Required for Printed Wiring Repair	6 - 81
7 - 1	Abbreviations	
7 - 2	Manufacturer Federal Supply Codes	
A - 1	Nonstandard Abbreviations	A - 1
B - 1	Radio Receiver R-1414/URR, Wire List	B - 1
B - 2	Counter A9, Wire List	B - 26
B - 3	AC Input Power Supply PS1, Wire List	B - 27
B - 4	DC Input Power Supply PS2, Wire List	B - 30

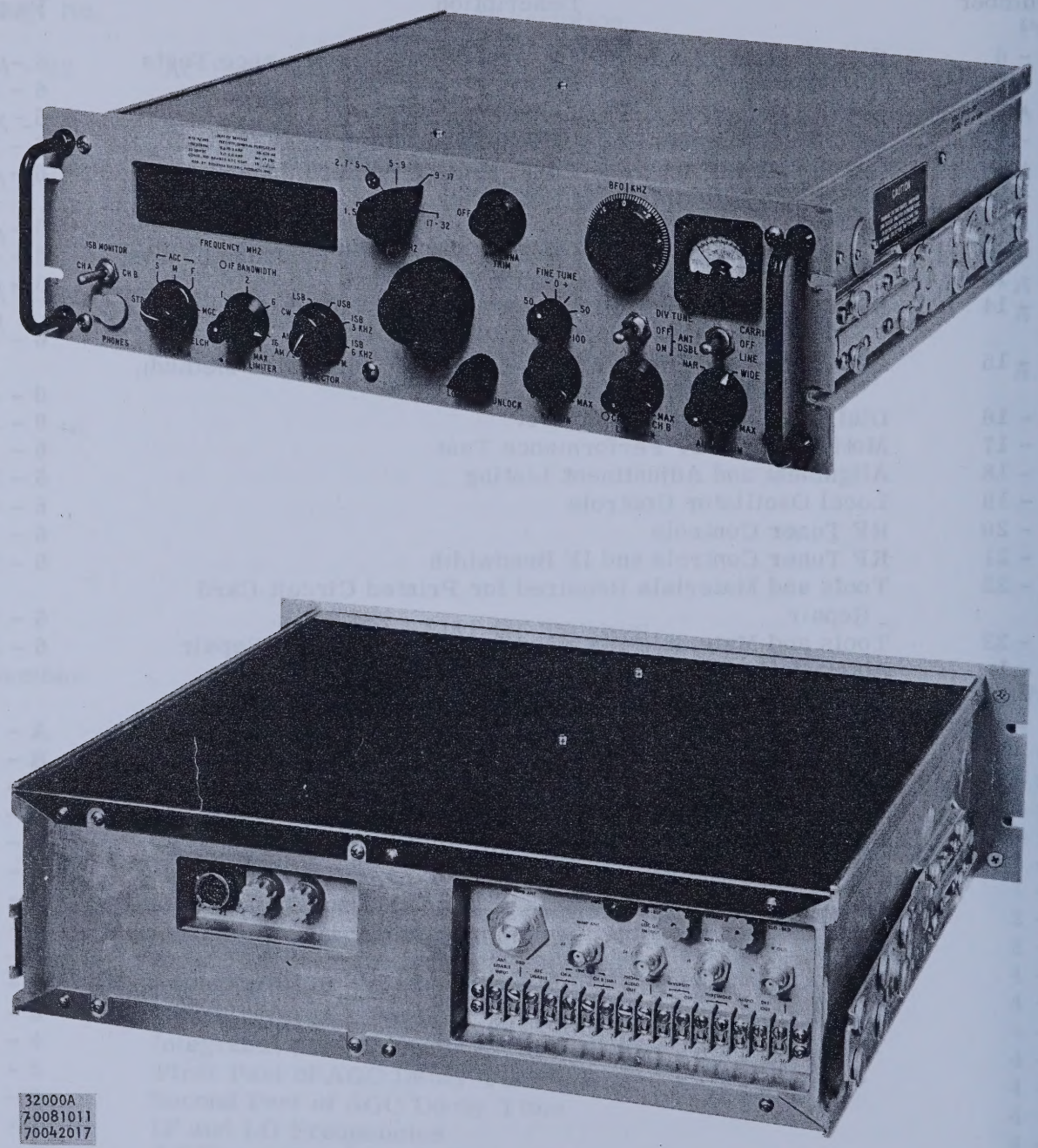


Figure 1-1. – R-1414/URR, HF General Purpose Radio Receiver.

CHAPTER 1

DESCRIPTION OF EQUIPMENT

1-1. GENERAL. - This chapter contains general information about the R-1414/URR, HF General Purpose Radio Receiver; such as classification, purpose, description, technical characteristics, and equipment supplied.

1-2. CLASSIFICATION. - The R-1414/URR, HF General Purpose Radio Receiver and this manual are unclassified (U).

1-3. PURPOSE AND DESCRIPTION. - The R-1414/URR Radio Receiver (see figure 1-1) is a solid-state, general purpose high frequency (HF) radio receiver covering the 1.5 to 32 MHz frequency range. It is intended primarily for operation in fixed stations or in transportable van stations when at a fixed station. The receiver is capable of detecting amplitude modulated (AM), continuous wave (CW), single sideband (SSB), independent sideband (ISB), frequency modulated (FM) signals, and frequency shifting keying (FSK) signals. Refer to table 1-1 for a listing of the emission types which can be received.

The receiver is a manually tuned superheterodyne type using dual conversion and employing an electronic counter readout with digital automatic frequency control (AFC). A basic feature is its frequency stability achieved by the internal digital AFC network and associated counter that has a front panel readout. Both frequency stability and readout accuracy are within ±50 Hz. When the receiver is not being tuned, the receiver's local oscillator is locked, via the counter, to a reference crystal oscillator that also serves as a time-base reference for the counter. Frequency stability and readout accuracy are essentially that of the crystal oscillator reference.

RF inputs to the receiver at a rear-panel can be received from low impedance (72 ohms) transmission lines at one input connector and from whip or random length antennas at the other input connector. IF and audio outputs are available at the rear-panel for use with auxiliary equipment. The receiver can be used with another receiver for diversity reception by use of the appropriate connections on the rear panel, as described in Chapter 2. A transmitter can use the same antenna by grounding the ANT DISABLE INPUT terminal on TB1 of the rear-panel and by operating the DIV TUNE-ANT DSBL switch on the front-panel to ON.

The primary structural units of the receiver are the front panel assembly and the main frame. The main frame is separated into four compartments which house the printed circuit cards for the RF section, counter section, the IF and audio section, and the power supply assembly. See figures 1-2 and 1-3 for top and bottom views of the receiver, identifying the major subassemblies. Refer to table 1-2 for a list of these subassemblies. The tuner capacitor assembly is located below the RF section at the bottom of the receiver. Most of the major subassemblies are slide-in type printed circuit boards; except for the following: power supply assembly, tuner sub-assembly, electrical RF connector assembly, BFO board, second local oscillator, filters, and the display board in the counter. The top of the receiver is covered with three separate RFI covers for the RF section, counter section, and IF and audio

Table 1-1. – Designation of Received Emissions.

TYPE OF MODULATION OF MAIN CARRIER	TYPE OF TRANSMISSION	SUPPLEMENTARY CHARACTERISTICS	SYMBOL	DETECTOR SWITCH POSITION
Amplitude Modulation	Telephony	Double sideband, full carrier	A3	AM
Amplitude Modulation	Telegraphy by the on-off keying of an amplitude-modulation audio frequency or audio frequencies, or by the on-off keying of the modulated emission (special case: an unkeyed emission amplitude modulated)	---	A2	AM
Amplitude Modulation	Telegraphy without the use of a modulation audio frequency (by on-off keying)	---	A1	CW or AM/BFO
Amplitude Modulation	Telephony	Single sideband, reduced carrier	A3a	LSB or USB
Amplitude Modulation	Telephony	Two independent sidebands, reduced carrier	A3b	ISB 3 kHz
Amplitude Modulation	Cases not covered by the above, such as a combination of telephony and telegraph	Two independent sidebands	A9b	ISB 6 kHz
Frequency (or phase) Modulation	Telegraphy by frequency-shift keying without use of a modulation audio frequency: one of two frequencies being emitted at any instant	---	F1	CW
Frequency (or phase) Modulation	Telephony	---	F3	FM

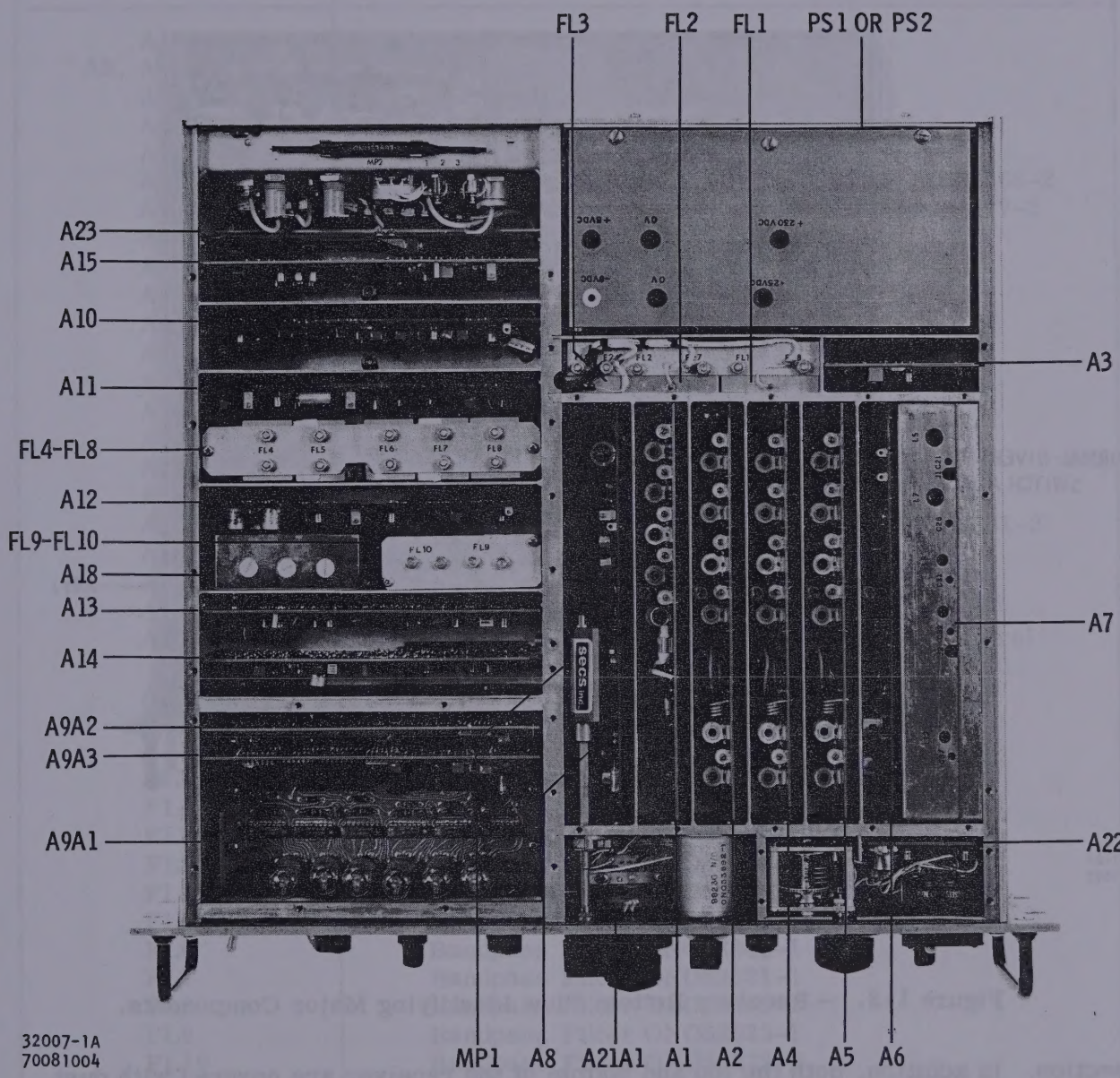


Figure 1-2. – Receiver Top View Identifying Major Components.

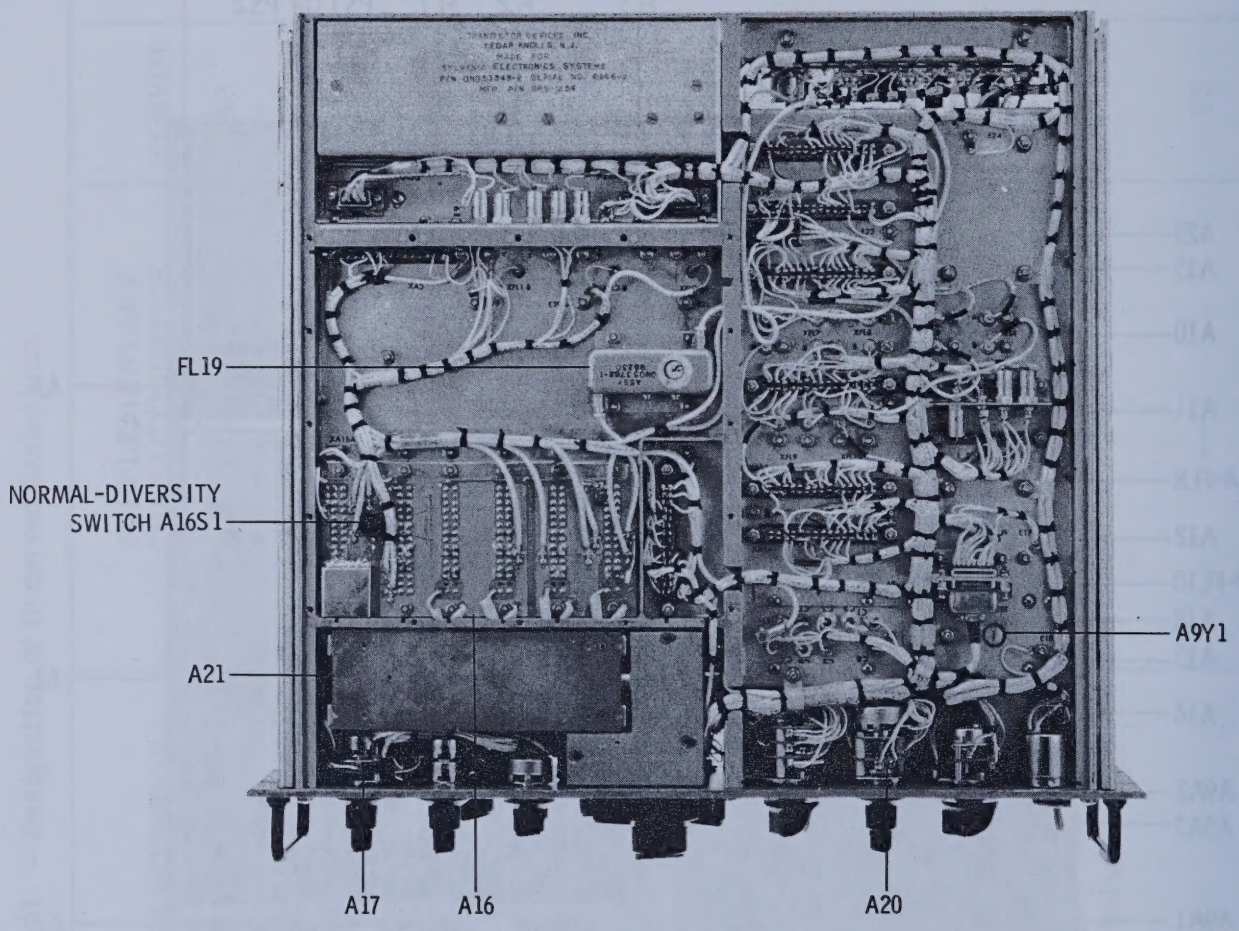


Figure 1-3. – Receiver Bottom View Identifying Major Components.

section. In addition, both the top and bottom of the receiver are covered with dust covers which completely enclose the two surfaces. The bottom dust cover also acts as a RFI cover for the RF section. The top and bottom dust covers are easily removable by sliding out towards the rear of the receiver. A slide drawer extension is provided with the receiver to allow for easy insertion or removal from a cabinet. The slide drawer extension also allows the receiver to be tilted up and down 45 degrees and 90 degrees.

Table 1-2. – Major Subassemblies.

REFERENCE DESIGNATOR	NAME
A1	Antenna Tuner ONO53556-2
A2, A4, A5	RF Tuner ONO53601-1
A3	RF Amplifier ONO53560-2
A6	First Mixer ONO53564-1
A7	First Local Oscillator ONO53576-1
A8	Automatic Frequency Control (AFC) ONO53568-2
A9	Electronic Digital Readout Counter ONO53577-2
A9A1	Display ONO53535-2
A9A2	Gate Generator ONO53539-1
A9A3	Divider ONO53543-1
A9Y1	1 MHz Oscillator ONO53327-1
A10	First IF Amplifier ONO53511-1
A11	Second Mixer ONO53515-2
A12	Second IF Amplifier ONO53593-2
A13	Detector ONO53519-2
A14	Independent Sideband (ISB) ONO53523-2
A15	AF Amplifier ONO53527-2
A16	Electrical RF Connector Assembly ONO53551-2
A17	Audio Switch and Gain Control ONO53805-1
A18	Second Local Oscillator ONO53382-2
A19	Not Used
A20	IF Bandwidth Switch and Noise Limiter Control ONO53367-2
A21	Tuner Subassembly ONO53644-2
A21A1	Motion Detector ONO53643-1
A22	BFO ONO53680-1
A23	Test Adapter ONO53674-1
FL1	Bandpass Filter ONO53324-1
FL2	Bandpass Filter ONO53325-1
FL3	Bandpass Filter ONO53326-1
FL4	Bandpass Filter ONO53318-1
FL5	Bandpass Filter ONO53319-1
FL6	Bandpass Filter ONO53345-1
FL7	Bandpass Filter ONO53321-1
FL8	Bandpass Filter ONO53409-1
FL9	Bandpass Filter ONO53323-1
FL10	Bandpass Filter ONO53323-2
FL19	Lowpass Filter ONO53762 -1
PS1	Power Supply ONO53349-2
PS2 (Optional)	Power Supply ONO53349-3
MP1	Gear Assembly ONO53399-2

1-4. TECHNICAL CHARACTERISTICS. - Table 1-3 lists the pertinent technical characteristics of the receiver.

1-5. EQUIPMENT SUPPLIED. - Table 1-4 lists the equipment and accessories supplied with the receiver.

1-6. EQUIPMENT REQUIRED BUT NOT SUPPLIED. - Table 1-5 lists the equipment required (or equivalent) for operation but not supplied as part of the receiver. Additional equipment may be required depending upon the receiver's use.

1-7. OPTIONAL EQUIPMENT. - Table 1-6 lists the optional equipment available for use with or in the receiver.

Table 1-3. – Technical Characteristics.

a. Frequency Range:

BAND	FREQUENCY RANGE
1	1.5-2.7 MHz
2	2.7-5 MHz
3	5-9 MHz
4	9-17 MHz
5	17-32 MHz

100 kHz overlap on all band edges.

b. Signal Detection capability:

AM (amplitude modulation)
CW (continuous wave)
USB (upper sideband) 3 kHz
LSB (lower sideband) 3 kHz
ISB (independent sideband) 3 kHz or 6 kHz
FM (frequency modulation)
AM/BFO with crystal BFO

c. Noise Figure:

Less than 10 db

d. Type of Frequency Control:

Manual tuning in 100 Hz increments using the main tuning control.
±100 Hz continuous tuning capability using the fine tuning control.

e. Frequency Readout Accuracy:

±50 Hz

Table 1-3. – Technical Characteristics –Continued.

f. Frequency Stability (at Audio Output with crystal BFO):

Short term – Less than ±5 Hz change during any 10-second period after 30-minute warmup

Long term – Less than ±15 Hz change during any 8-hour period after a 4-hour warmup

Temperature – Less than 30 Hz change for temperature changes of 10°C anywhere within the range of 0° to 60°C

g. Image, IF, and Spurious Rejection:

80 db or greater

h. Incidental FM:

Less than ±5 Hz rms deviation

i. IF Frequencies; Dual Conversion:

BAND	FIRST IF	SECOND IF
1	392 kHz	455 kHz
2 and 3	762 kHz	455 kHz
4 and 5	2.762 MHz	455 kHz

(1) IF bandwidth characteristics:

IF BW SWITCH SETTING	MINIMUM 3 db BANDWIDTH	MAXIMUM 60 db BANDWIDTH
0.1 kHz	0.1 kHz	1.0 kHz
1 kHz	1.0 kHz	3.3 kHz
2 kHz	2.0 kHz	5.5 kHz
6 kHz	6.0 kHz	13.0 kHz
16 kHz	16.0 kHz	32.0 kHz

(2) IF Output (455 kHz):

Greater than 20 millivolts rms across 50 ohms, with 3 microvolts rms of RF input

(3) BFO: 455 kHz oscillator

(4) BFO Control: Adjustable ±8 kHz

Table 1-3. – Technical Characteristics –Continued.

j. Audio Output Signals:

With 3.0 microvolts rms RF input, minimum audio output into 600 ohms at the line output is 1.0 mw and at the headphone output is 50 mw. Frequency response is within ±1.5 db from 100 Hz to 15 kHz. The headphone output has an optional 3.5 kHz low-pass filter (medium bandwidth).

k. Automatic Gain Control:

Audio output level increase is less than 3 and 4 db when input signal level is increased from 10 microvolts rms to 30,000 and 100,000 microvolts rms respectively.

l. Input Impedance:

Low Impedance Antenna – 72 ohms, nominal, VSWR less than 2:1
Whip Antenna – Variable (ANTENNA TRIM on)

m. Power Requirements:

110 VAC (±15%), 60 watts, maximum, 48-420 Hz
220 VAC (±15%), 60 watts, maximum, 48-420 Hz
+22 to +30 VDC, 60 watts, maximum (with ONO53349-3 power supply)

n. Antenna Input Circuit Protection:

(1) Automatic protection for RF signal power greater than +15 dbm
(2) Manual protection (relay, greater than 60 db attenuation) for operation of the receiver with a transmitter

o. Diversity Reception:

(1) Rear panel LOC OSC connection for the variable frequency injection used by the frequency conversion circuits
(2) Rear panel adjustment of the AGC voltage to allow AGC tracking between receivers

p. Squelch: Approximately 20 db quieting (internal adjustable threshold)

q. Noise Limiter: Adjustable

r. Environmental Conditions:

(1)	Operating Temperature	0°C to +60°C (32°F to 140°F)
(2)	Relative Humidity	0 to 100 percent
(3)	Altitude	
	Operating	Up to 12,000 feet
	Non-operative	Up to 50,000 feet
(4)	Storage Temperatures	-62°C to +75°C (-79.6°F to +167°F)

Table 1-4. – Equipment Supplied.

ITEM	WEIGHT	DIMENSIONS	GENERAL DESCRIPTION
R-1414/URR, HF General Purpose Radio Receiver	49 lbs	5.22 x 18.13 x 19 inches	Superheterodyne, dual-conversion receiver employing a counter readout and digital AFC
Extension Drawer Slide ONO53374	1 lb	0.44 x 3.25 x 13.5 inches	Standard extension drawer slides that will be affixed to the receiver to allow easy removal from cabinet.
AC Power Cable ONO53370-1	1 lb	Length 6 feet	Connects receiver to 110 VAC power source

Table 1-5. – Equipment Required But Not Supplied.

ITEM	GENERAL DESCRIPTION
Antenna	
Unbalanced	Antenna having a 72 ohm coaxial output
Whip	A whip antenna having a length of approximately 12 feet.
Audio Reproducer	Headset or loudspeaker. Any audio interface device designed for 600 ohms impedance (either balanced or unbalanced) and 50 mw power input.
Mounting and Housing Facilities	Rack, console, or equipment cabinet designed for standard 19 inch width and for mounting slide equipped receiver. Necessary brackets and angle adaptors must be provided for proper interface between slide and cabinet.

Table 1-6. – Optional Equipment.

ITEM	WEIGHT	DIMENSIONS	GENERAL DESCRIPTION
Power Supply PS2 (DC Input) ONO53349-3	5 lb	8.49 by 4.47 by 4.16 inches	This is a dc input (+22 to +30 vdc) power supply that is used to replace the ac input power supply when only a dc power source is available.
Bandpass Filter ONO53359-1	0.1 lb	3.440 by 1.260 by 1.050 inches	This is a 3.5 kHz bandwidth filter at 3 db down, that may be used to replace the 2 kHz bandwidth filter FL6.
Bandpass Filter ONO53322-1	0.1 lb	3.440 by 1.260 by 1.050 inches	This is a 3.0 kHz min. to 3.5 kHz max. bandwidth filter at 3 db down with precision time delay within ±25 μsec. May be used to replace the 2 kHz bandwidth filter FL6.
Electrical Power Cable Assembly ONO53370-2	0.1 lb	Approximately 6 ft in length	Provides connection for dc input power supply ONO53349-3 to a dc power source.

CHAPTER 2

INSTALLATION

2-1. GENERAL. - This chapter contains instructions for installing and conditioning the receiver for operation.

WARNING

HIGH VOLTAGE (SPECIFICALLY +230 VDC) IS PRESENT AT OUTPUT OF POWER SUPPLY PS1 AND IN COUNTER A9. EITHER DISCONNECT POWER OR BE EXTREMELY CAUTIOUS WHEN WORKING ON RECEIVER WITH THE DUST AND RFI COVERS REMOVED. CONTACT WITH THIS VOLTAGE COULD RESULT IN INJURY TO PERSONNEL.

2-2. SITE SELECTION. - The receiver can be used in fixed or transportable van stations where the following power and antenna requirements are available:

a. Power Requirements:

(1) 110 vac (±15%), 48 to 420 Hz, 60 watts maximum } (with power supply
(2) 220 vac (±15%), 48 to 420 Hz, 60 watts maximum } ONO53349-2)
(3) 22 to 30 vdc, 60 watts maximum (with power supply ONO53349-3)

b. Antenna Requirements:

(1) LOW IMPD ANT connector J2 is a type C receptacle that is provided for connection to low impedance coaxial transmission lines. Input impedance is 72 ohms. Any type antenna can be used provided the output is 72 ohms unbalanced.

(2) WHIP ANT connector J3 is a BNC type receptacle that is provided for connection to whip and random length type antennas.

2-3. INSTALLATION PROCEDURES.

a. Placement and Mounting. - The receiver is normally mounted in a standard 19-inch electrical equipment cabinet. Refer to figure 2-1 for an interface drawing of the receiver and the slide drawer extension. Using the dimensions shown in figure 2-1 the appropriate cabinet adaptors can be installed by the user for proper interface with the receiver or with a receiver with slide drawer extensions. There should be sufficient room to the rear of the receiver for installation of the input, output, and control cables, and for access to the rear panel. All RFI and dust covers should remain on the receiver and the covers should be securely fastened with all mounting screws, except when the receiver is being serviced. After the electrical equipment cabinet has been conditioned, the receiver may then be installed.

(1) Receiver with Slide Drawer Extensions. - The cabinet section of the slide drawer extension (see figure 2-2) must first be installed in the cabinet using six mounting screws. The receiver, with the chassis section of the slide drawer extension mounted, is then mated with the cabinet section of the slide drawer extension. The receiver can be pushed partially into the cabinet after pressing the release button on each chassis section of the slide drawer extensions. Two locking devices located on the inside of the cabinet mounted slide drawer extension must be pulled up or down to allow the receiver to be completely inserted into the cabinet. Four mounting screws must be used to secure the receiver to the cabinet. The necessary room needed when removing the slide-out type dust covers can be provided by pulling the receiver out of cabinet to full extent of the slide drawer extension travel, then pull release lever and tilt the receiver 90 degrees up or down.

(2) Receiver without Slide Drawer Extensions. - Ensure that the proper cabinet adaptors have been installed to support the rear of the receiver. Insert the receiver into the cabinet until the rear of the receiver interfaces with the cabinet adaptors. Secure the receiver to the cabinet with four mounting screws at the front panel.

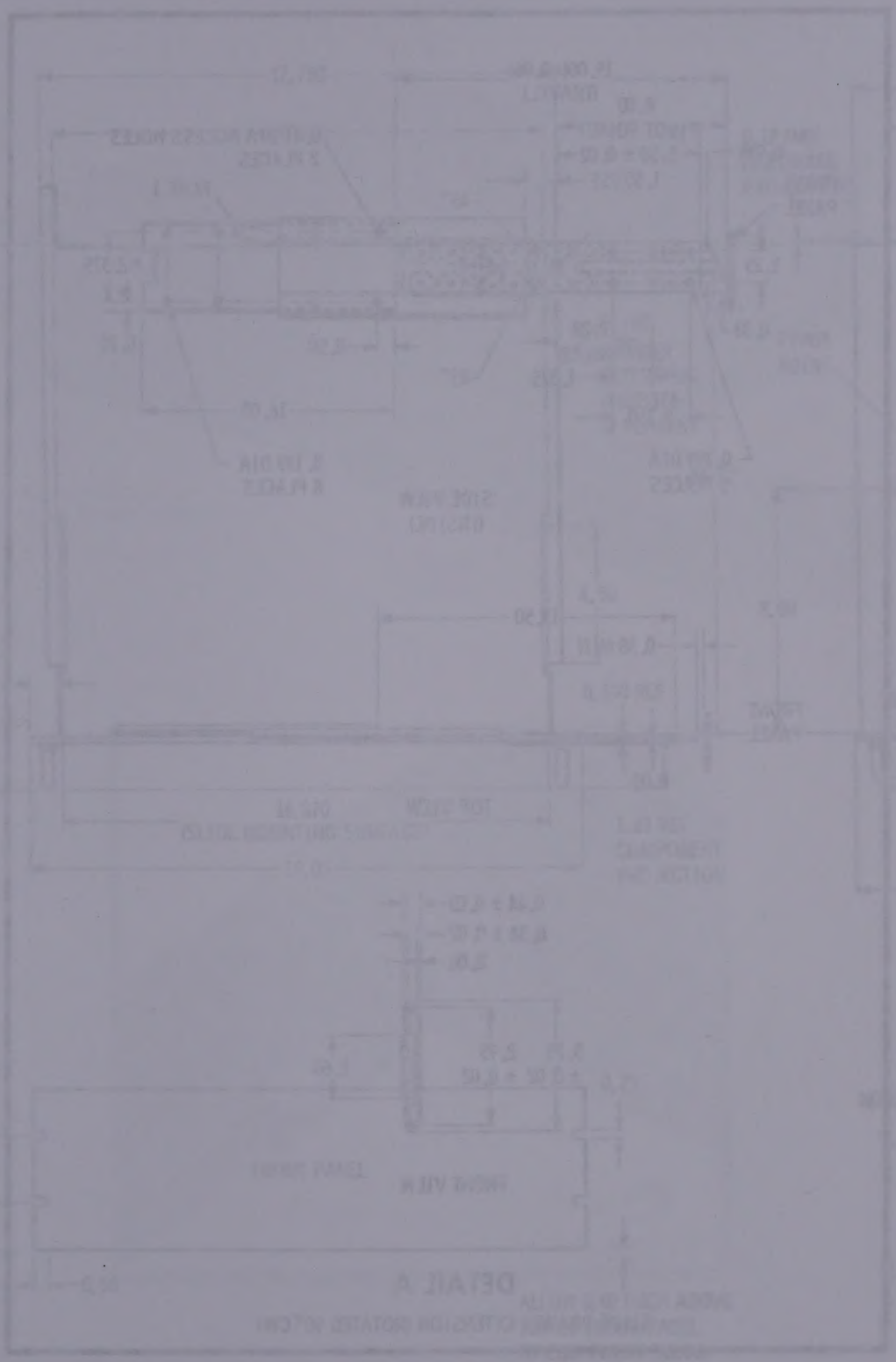
b. Power Cables. - A different power cable must be used for each of the three input sources. In the event a power cable is not available, refer to figure 2-3 and fabricate the appropriate cable as shown in the diagram.

c. Rear-Panel Connections and Controls. - Refer to figure 2-4 for the location of the connectors and controls listed in table 2-1.

d. Single-receiver Operation. - When using a single receiver to receive signals, connect the equipment as shown in figure 2-5. Attach the system ground to TB1-9, using a heavy grounding wire.

e. Diversity Operation. - When using the two receivers in diversity operation, connect the equipment as shown in figure 2-6. Attach the system ground to TB1-9 of each receiver, using a heavy grounding wire.

2-4. INITIAL CHECKOUT AND ADJUSTMENTS. - An operational checkout of the receiver can be made by conducting the performance test procedures in table 5-3 of chapter 5. These are minimum performance test standards for the receiver that are performed on a scheduled basis as detailed in chapter 5. If these tests indicate the receiver is not performing properly, refer to chapter 6 and conduct the performance test standards and/or the alignment procedures.



(1) Receiver with Slide Drawer Extensions. - The cabinet section of the slide drawer extension (see figure 2-2) must first be installed in the cabinet using six mounting screws. The receiver, with the chassis section of the slide drawer extension mounted, is then mated with the cabinet section of the slide drawer extension. The receiver can be pushed partially into the cabinet after pressing the release button on each chassis section of the slide drawer extensions. Two locking devices located on the inside of the cabinet mounted slide drawer extension must be pulled up or down to allow the receiver to be completely inserted into the cabinet. Four mounting screws must be used to secure the receiver to the cabinet. The necessary room needed when removing the slide-out type dust covers can be provided by pulling the receiver out of cabinet to full extent of the slide drawer extension travel, then pull release lever and tilt the receiver 90 degrees up or down.

(2) Receiver without Slide Drawer Extensions. - Ensure that the proper cabinet adaptors have been installed to support the rear of the receiver. Insert the receiver into the cabinet until the rear of the receiver interfaces with the cabinet adaptors. Secure the receiver to the cabinet with four mounting screws at the front panel.

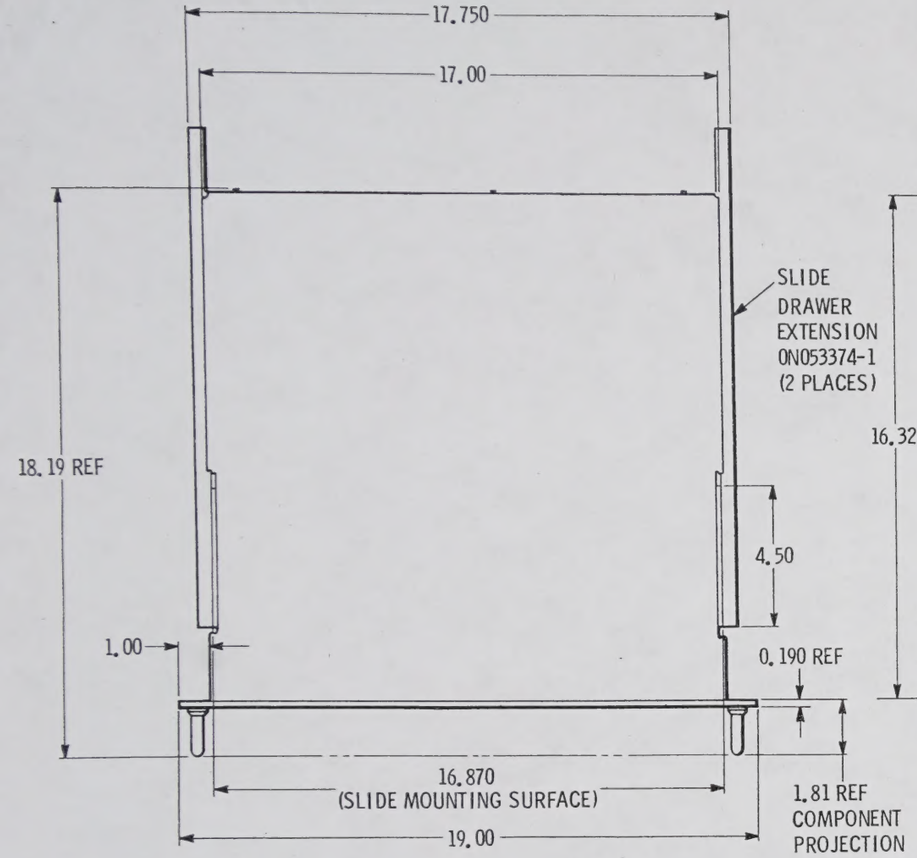
b. Power Cables. - A different power cable must be used for each of the three input sources. In the event a power cable is not available, refer to figure 2-3 and fabricate the appropriate cable as shown in the diagram.

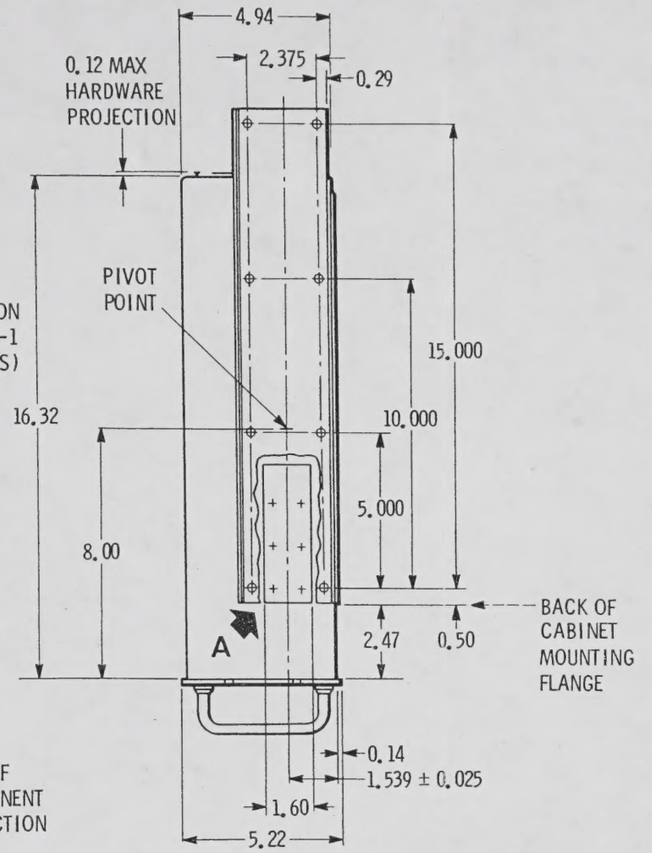
c. Rear-Panel Connections and Controls. - Refer to figure 2-4 for the location of the connectors and controls listed in table 2-1.

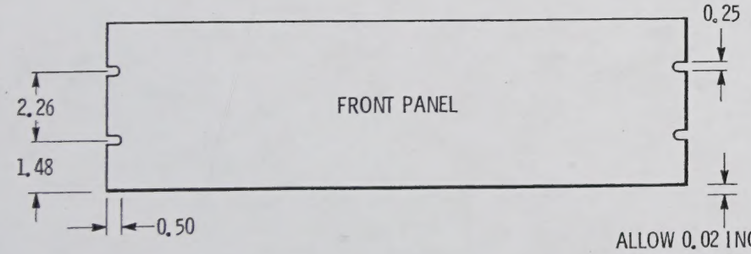
d. Single-receiver Operation. - When using a single receiver to receive signals, connect the equipment as shown in figure 2-5. Attach the system ground to TB1-9, using a heavy grounding wire.

e. Diversity Operation. - When using the two receivers in diversity operation, connect the equipment as shown in figure 2-6. Attach the system ground to TB1-9 of each receiver, using a heavy grounding wire.

2-4. INITIAL CHECKOUT AND ADJUSTMENTS. - An operational checkout of the receiver can be made by conducting the performance test procedures in table 5-3 of chapter 5. These are minimum performance test standards for the receiver that are performed on a scheduled basis as detailed in chapter 5. If these tests indicate the receiver is not performing properly, refer to chapter 6 and conduct the performance test standards and/or the alignment procedures.



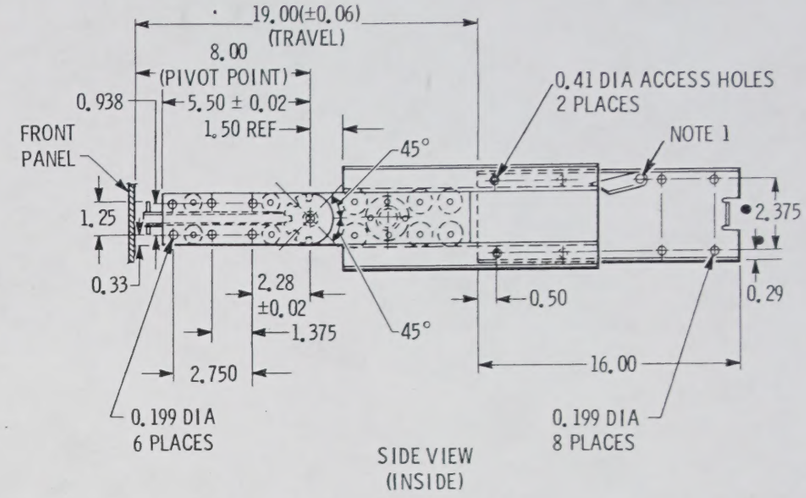




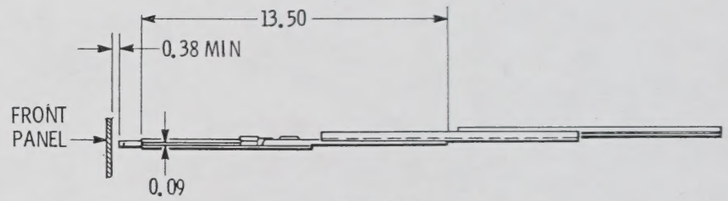
32003

NOTES:

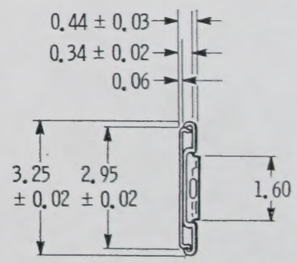
1. LOCK WILL BE LOCATED ON TOP SIDE WHEN USED AS A LEFT HAND SLIDE AND ON THE BOTTOM SIDE WHEN USED AS A RIGHT HAND SLIDE
2. ALL 2 PLACE DIMENSIONS ARE ± 0.03 AND 3 PLACE DIMENSIONS ARE ± 0.010 UNLESS OTHERWISE SPECIFIED



SIDE VIEW (INSIDE)



TOP VIEW



FRONT VIEW

DETAIL A

SLIDE DRAWER EXTENSION (ROTATED 90° CW)

Figure 2-1. - Receiver Interface Drawing

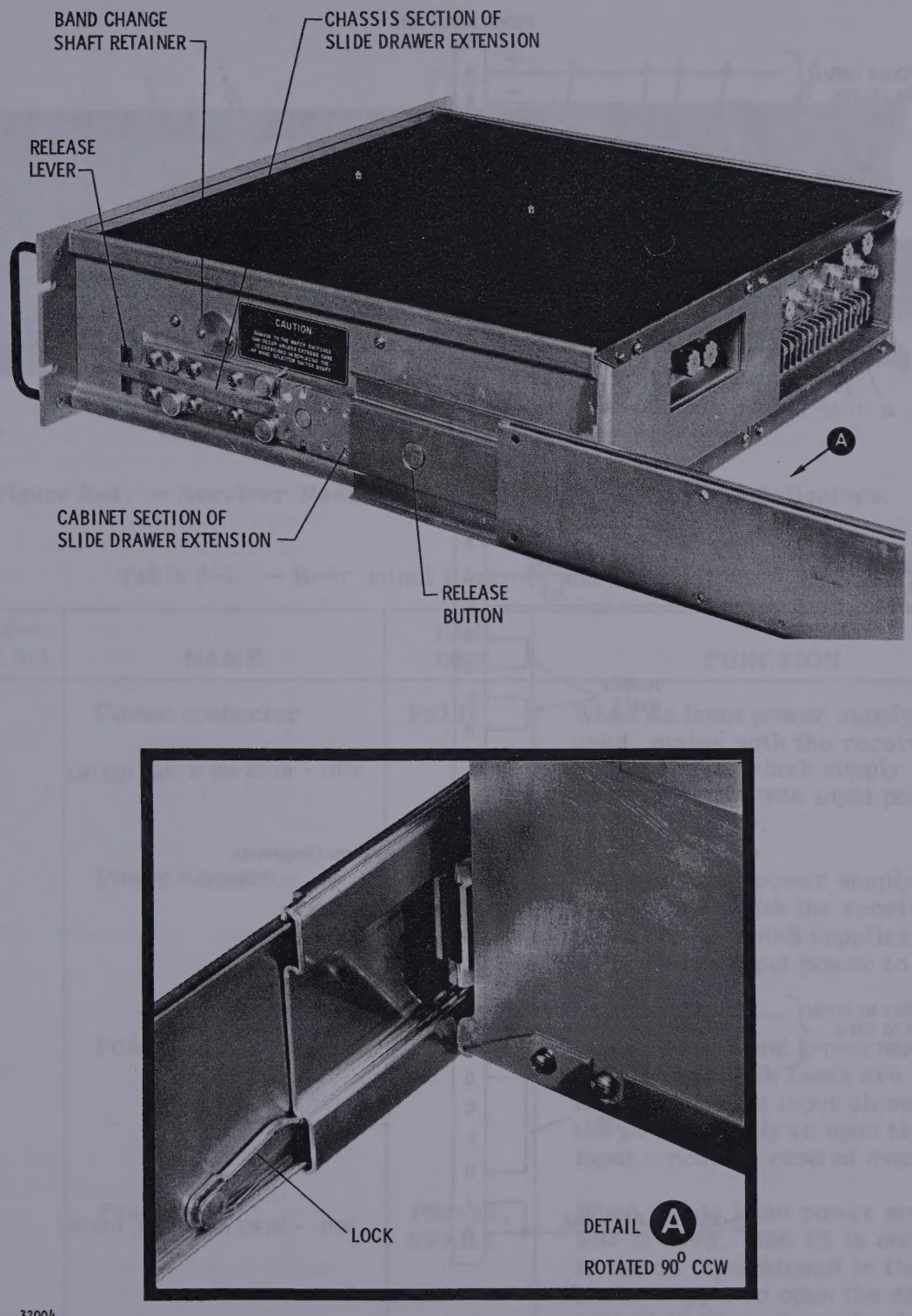
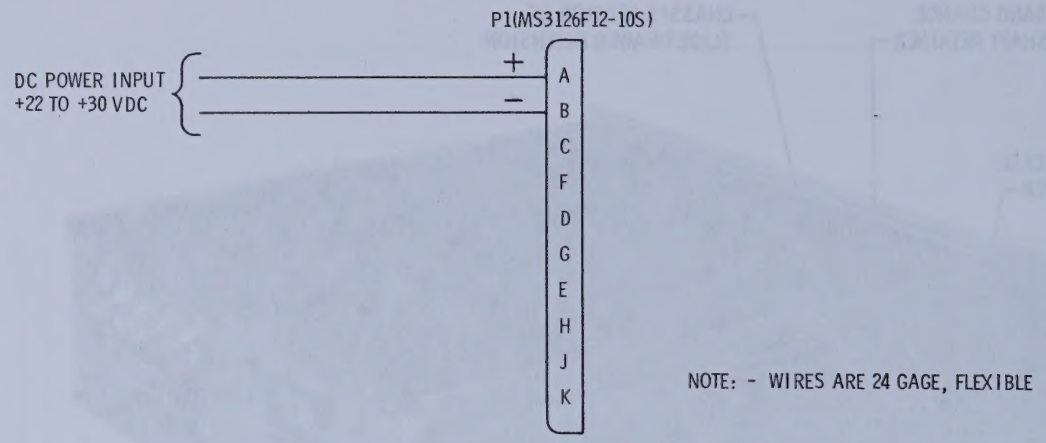
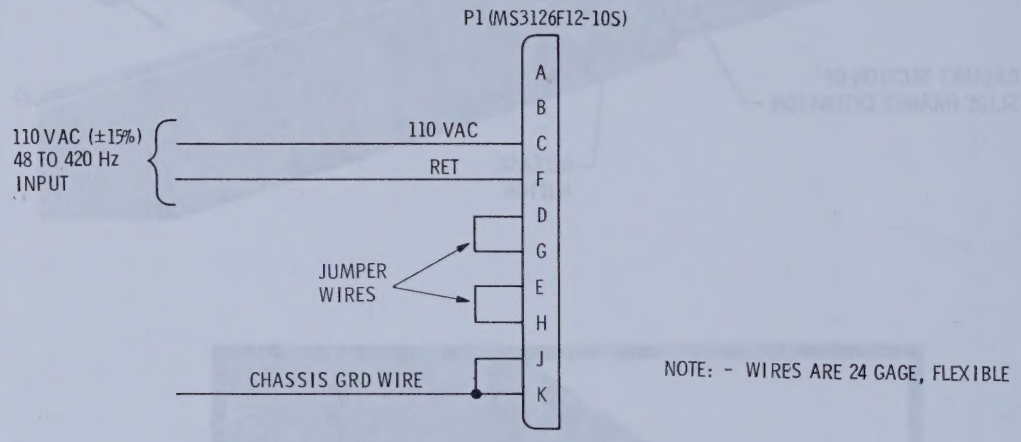


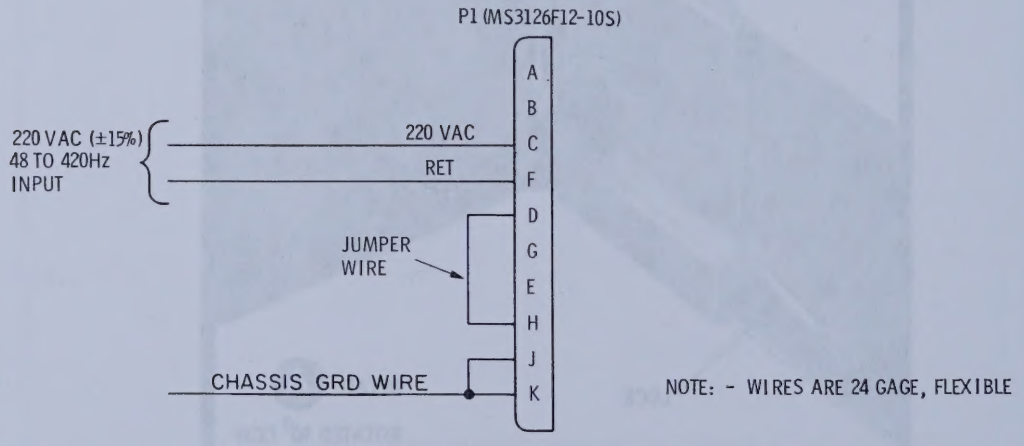
Figure 2-2. – Receiver with Slide Drawer Extension.



A. DC Power Cable Schematic and Components.



B. 110 VAC Power Cable Schematic and Components.



C. 220 VAC Power Schematic and Components.

32009A

Figure 2-3. – Power Cable Schematics.

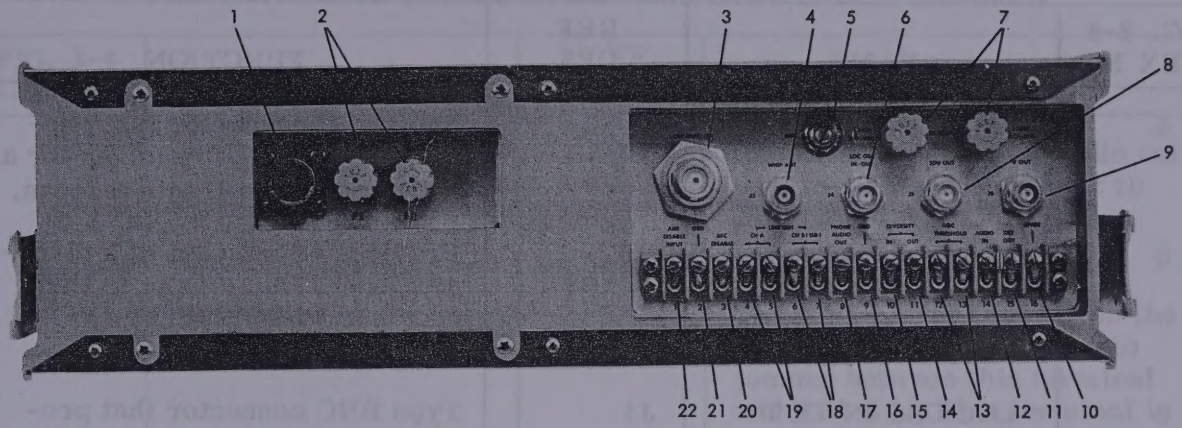


Figure 2-4. – Receiver Rear View, Identifying Controls and Indicators.

Table 2-1. – Rear Panel Controls and Connections.

FIG. 2-4 INDEX NO.	NAME	REF. DES.	FUNCTION
1	Power connector	PS1J1	When ac input power supply is used, mates with the receiver power cables which supply 115 vac or 220 vac input power to the receiver.
	Power connector	PS2J1	When dc input power supply is used, mates with the receiver power cable which supplies 22 to 30 vdc input power to the receiver.
2	Fuse	PS1-F1, F2	When the ac input power supply PS1 is used both fuses are connected in the ac input circuit to the power supply to open the ac input circuit in case of overload.
	Fuses	PS2-F1, SPARE	When the dc input power supply PS2 is used, fuse F1 is connected in the dc input circuit to the power supply to open the dc input circuit in case of overload. The other fuse is a spare.
3	LOW IMPD ANT connector	J2	Type C connector that provides 72-ohm input to the receiver for a coaxial transmission line.

Table 2-1. – Rear Panel Controls and Connections -Continued.

FIG. 2-4 INDEX NO.	NAME	REF. DES.	FUNCTION
4	WHIP ANT connector	J3	Type BNC connector that provides input to the receiver for a whip or random length antenna.
5	AGC control	R6	Provides adjustment of a diversity AGC voltage input to the receiver at DIVERSITY IN terminal TB1-10.
6	LOC OSC IN/OUT connector	J4	Type BNC connector that provides LO input from an external oscillator or LO output from receiver. These LO inputs or outputs are used when two receivers are connected for diversity operation. Control of the LO input/output is provided by a diversity switch A16S1 at the bottom (see figure 1-3) of the chassis on the RF section connector assembly A16. The LO frequencies are as follows: BAND 1: 1.892 to 3.092 MHz BAND 2;3: 3.462 to 9.762 MHz BAND 4,5: 11.762 to 34.762 MHz
7	SPARE fuses, 1 AMP SLO-BLO		Two spare one ampere slow-blow type fuses.
8	SDU OUT connector	J5	Type BNC connector that provides 455 kHz second IF output from receiver for interface with a spectrum display unit.
9	IF OUT connector	J6	Type BNC connector that provides 455 kHz second IF output from receiver.
10	SPARE terminal	TB1-16	Spare terminal board connection.
11	DET OUT terminal	TB1-15	Provides detected audio output from the AM, CW, USB, LSB, and FM detector stages of the receiver. Normally jumpered directly to the AUDIO IN terminal TB1-14.

Table 2-1. – Rear Panel Controls and Connections -Continued.

FIG. 2-4 INDEX NO.	NAME	REF. DES.	FUNCTION
12	AUDIO IN terminal	TB1-14	Receives the detected audio output from TB1-15 for input to audio amplifiers.
13	AGC THRESHOLD terminals	TB1-12	Lowers AGC threshold. Threshold level depends on the value of the resistor used to jumper between this terminal and TB1-13. This terminal is normally open.
		TB1-13	Provides -8 volts, which is jumpered, through a resistor, to TB1-12. This lowers the AGC threshold. This terminal is normally open.
14	DIVERSITY OUT terminal	TB1-11	Provides AGC output to another receiver when two receivers are connected for diversity operation.
15	DIVERSITY IN terminal	TB1-10	Provides AGC input from another receiver when two receivers are connected for diversity operation.
16	GRD terminal	TB1-9	Provides a receiver ground connection. Normally connected to a facility grounding wire.
17	PHONE AUDIO OUT terminal	TB1-8	Provides rear-panel access to unbalanced phone audio output. Parallels the PHONES audio output at the front panel.
18	LINE OUT CH B (ISB) terminals	TB1-6,7	Provides balanced line LSB audio output from the receiver's channel B when in ISB mode.
19	LINE OUT CH A terminals	TB1-4,5	Provides balanced line audio output from the receiver's channel A (in ISB mode, these terminals provide USB audio).
20	AFC DISABLE terminal	TB1-3	Manually disables the receiver AFC circuit when the terminal is grounded.

Table 2-1. – Rear Panel Controls and Connections -Continued.

FIG. 2-4 INDEX NO.	NAME	REF. DES.	FUNCTION
21	GRD terminal	TB1-2	Provides a ground connection that may be easily jumpered to TB1-3 and TB1-1.
22	ANT DISABLE INPUT terminal	TB1-1	The antenna circuits and the RF amplifier A3 can be disabled remotely when the DIV TUNE-ANT DSBL switch S4 is set to ON by switching TB1-1 to ground.

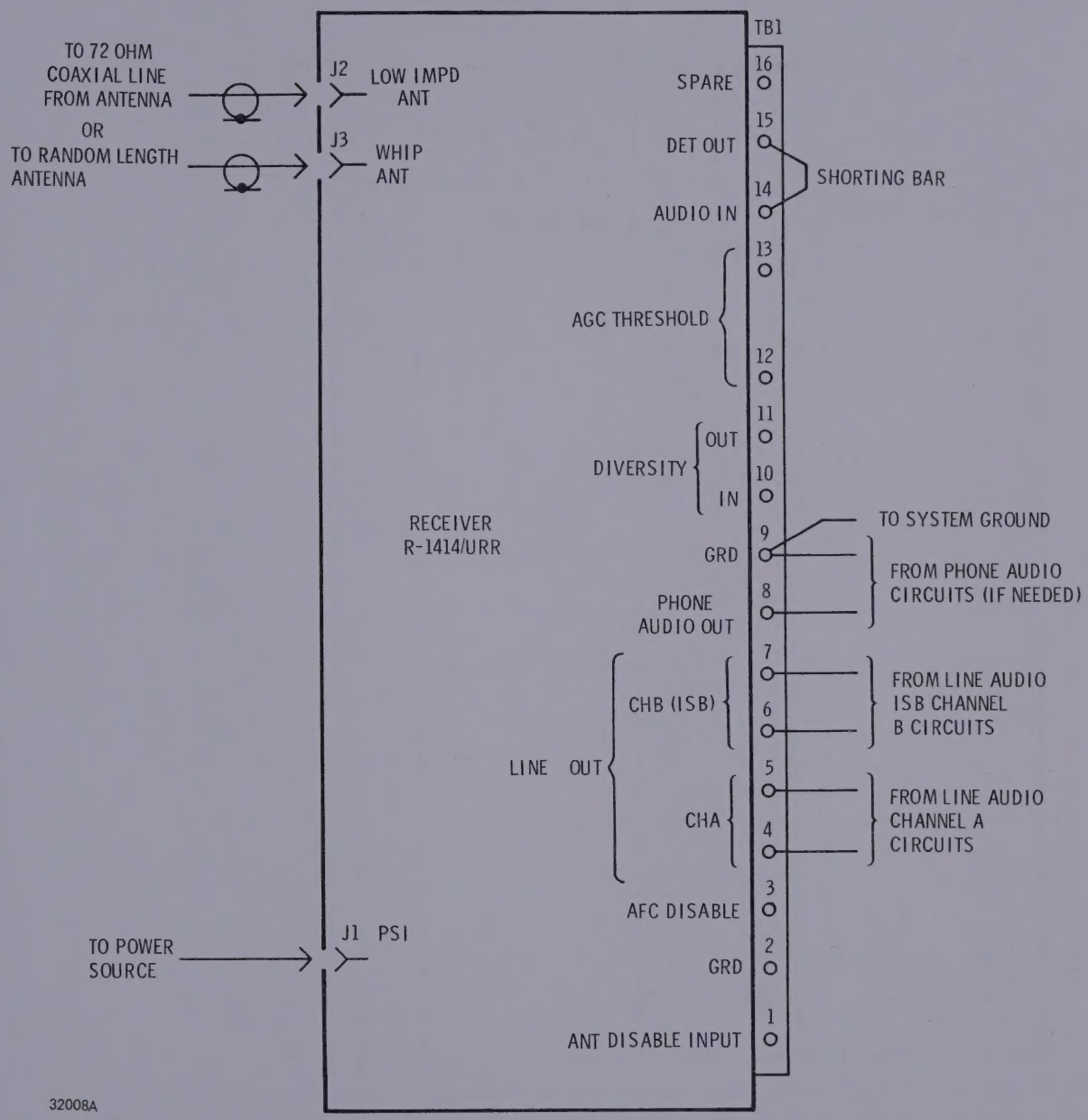
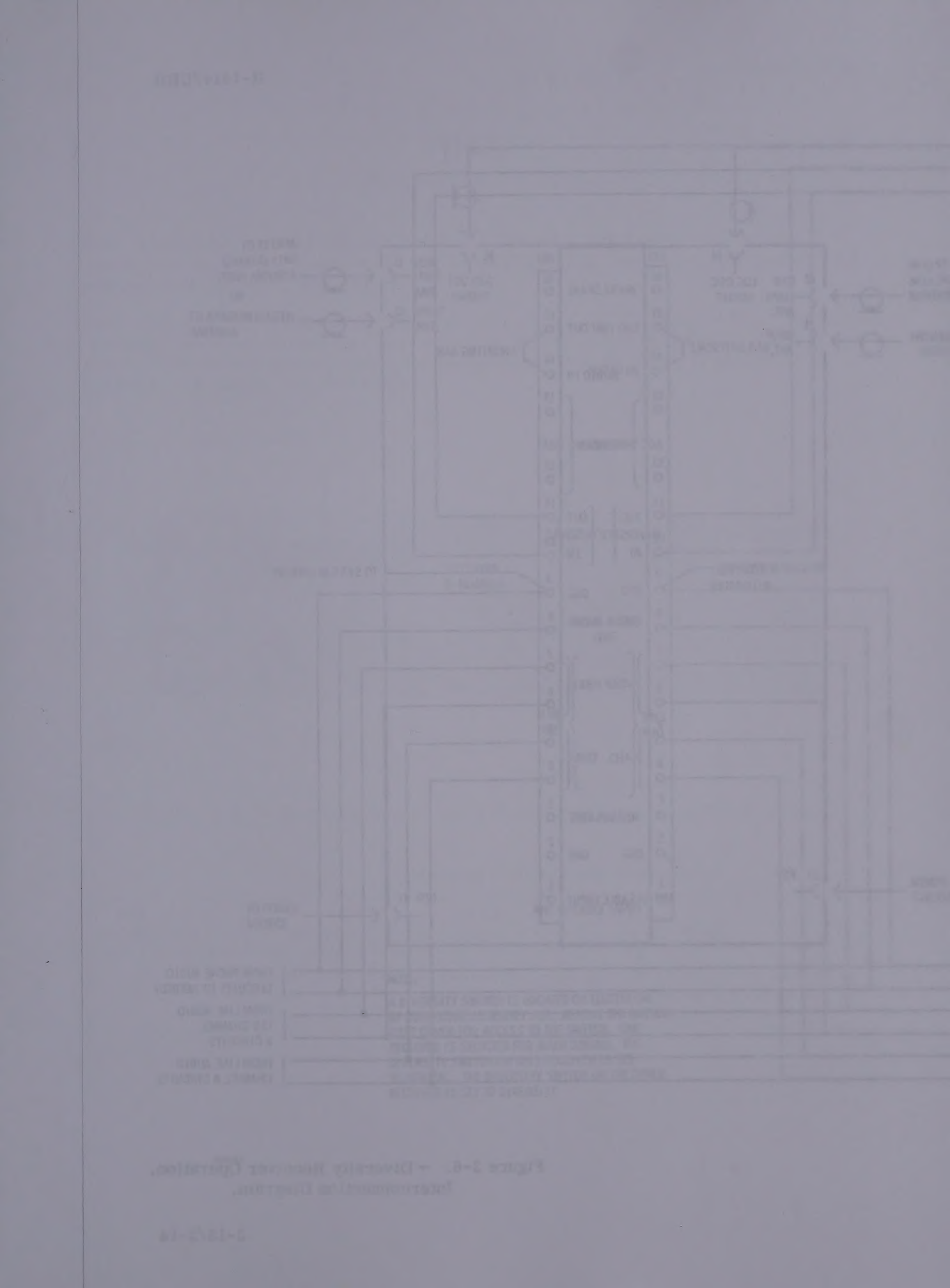
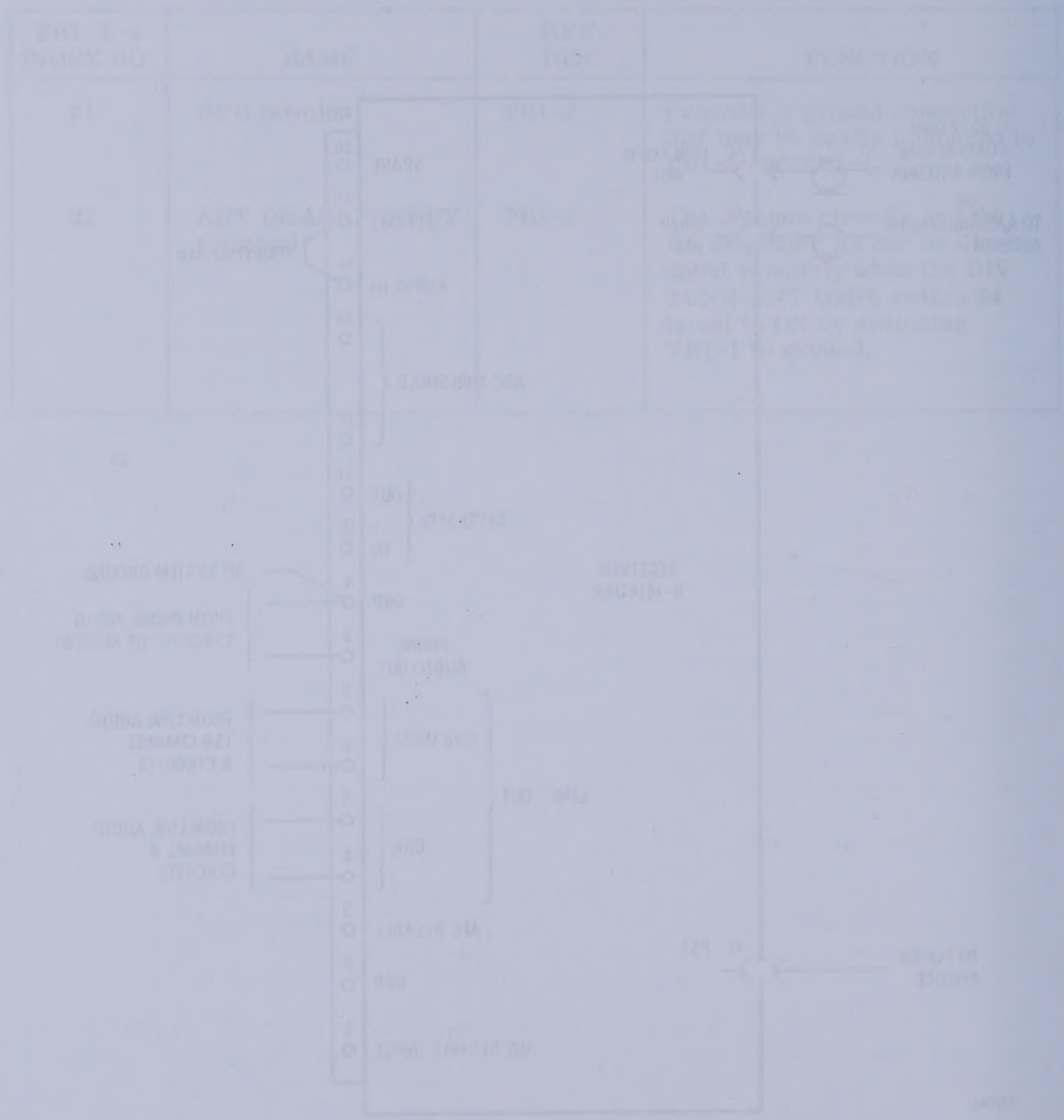
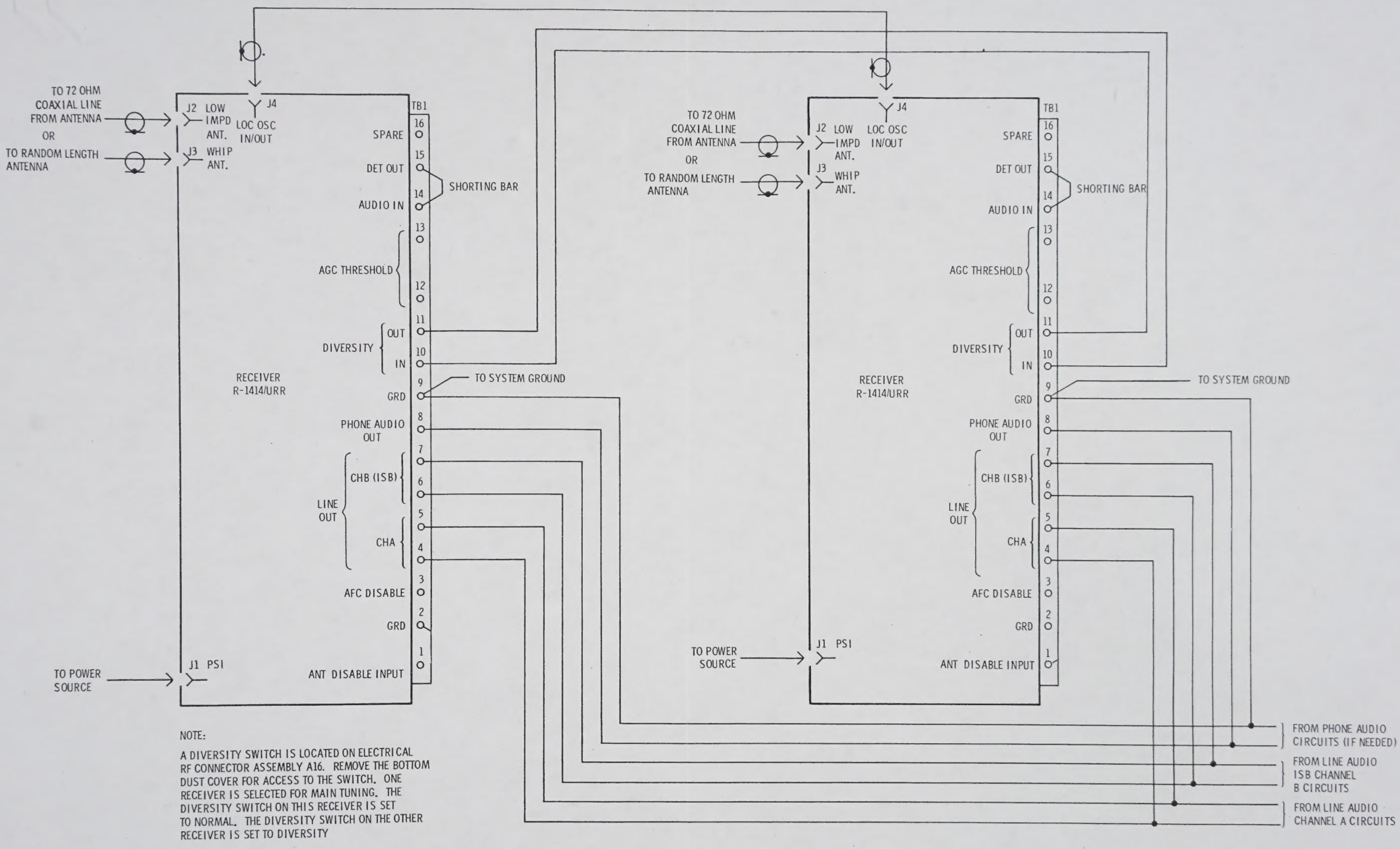


Figure 2-5. – Single Receiver Operation, Interconnection Diagram.





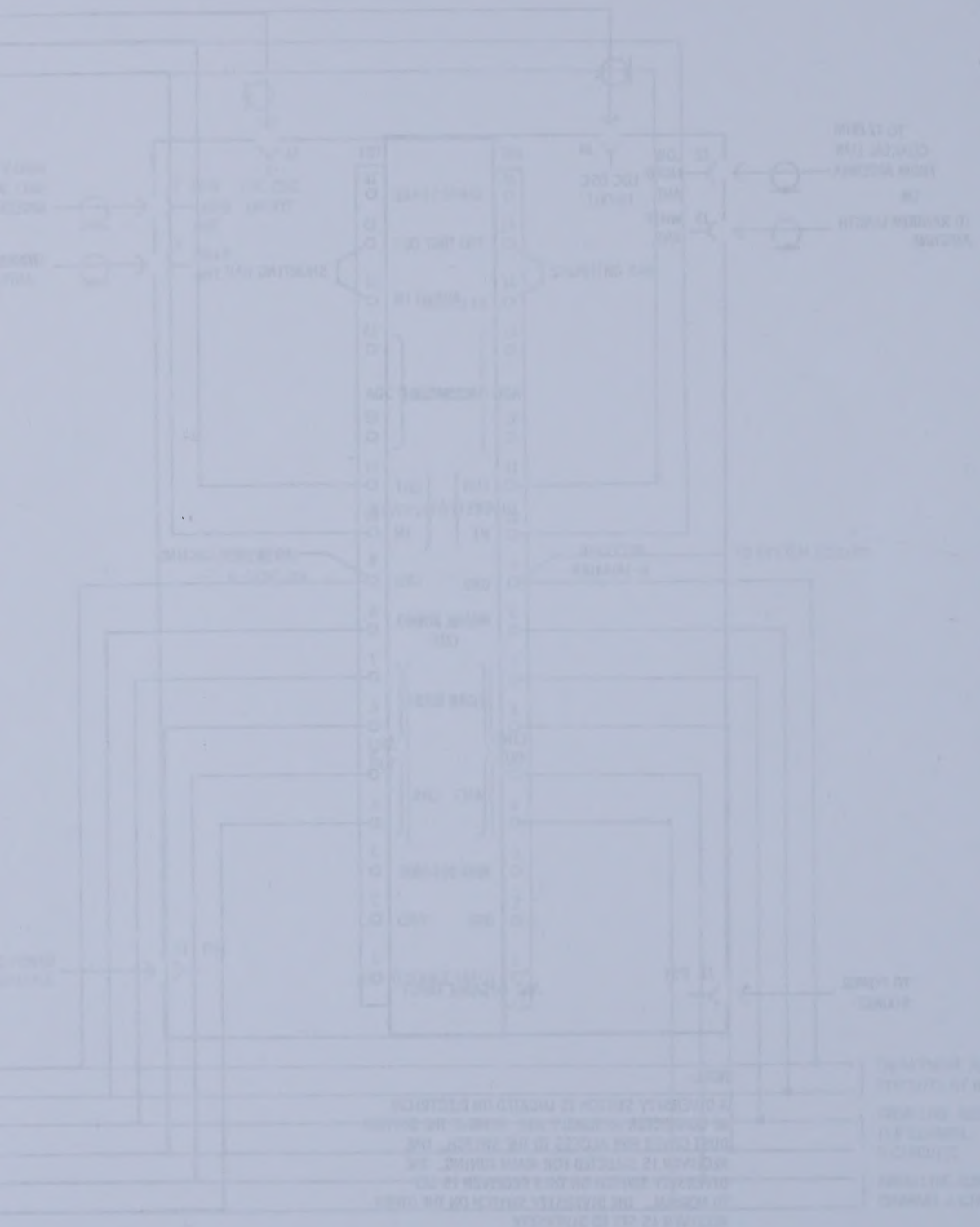


NOTE:

A DIVERSITY SWITCH IS LOCATED ON ELECTRICAL RF CONNECTOR ASSEMBLY A16. REMOVE THE BOTTOM DUST COVER FOR ACCESS TO THE SWITCH. ONE RECEIVER IS SELECTED FOR MAIN TUNING. THE DIVERSITY SWITCH ON THIS RECEIVER IS SET TO NORMAL. THE DIVERSITY SWITCH ON THE OTHER RECEIVER IS SET TO DIVERSITY

32005A

Figure 2-6. – Diversity Receiver Operation, Interconnection Diagram.



CHAPTER 3

OPERATING INSTRUCTIONS

3-1. GENERAL. - This chapter contains information and instructions needed to operate the receiver. It describes and locates controls, indicators, and connectors, and provides operating procedures.

3-2. OPERATING CONTROLS, INDICATORS, AND CONNECTOR. - The location of operating controls, indicators, and connector is provided in figure 3-1. Table 3-1 details front panels names, reference designations, and functions of operating controls, indicators, and connector.

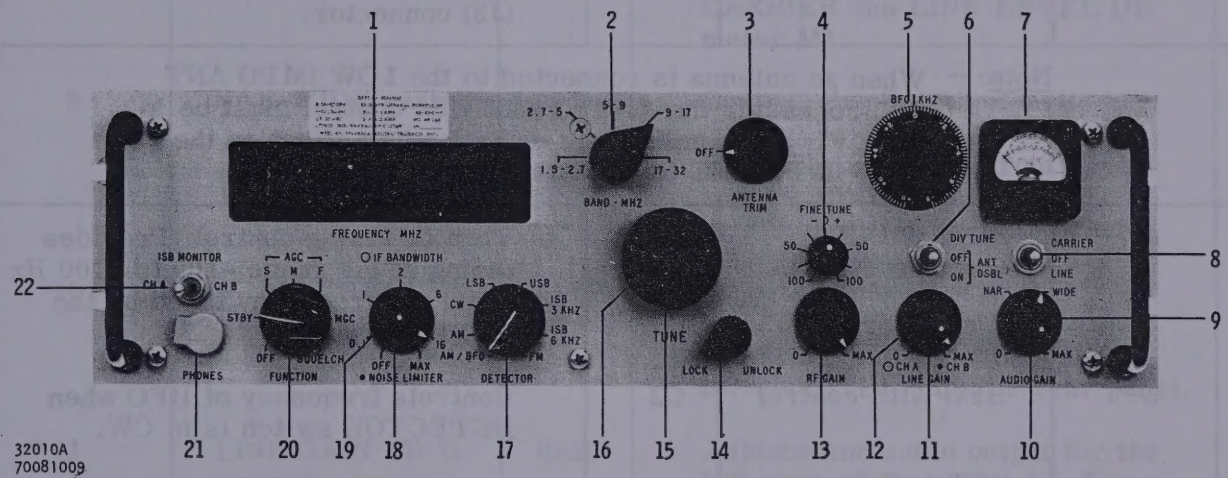


Figure 3-1. – Receiver Front Panel, Operating Controls, and Indicators.

Table 3-1. – Operating Controls and Indicators.

FIG. 3-1 INDEX NO.	NAME	REF. DES.	FUNCTION
1	FREQUENCY MHZ display	A9A1DS1 through A9A1DS6	Six display tubes visible through the front panel provide readout of frequency to which receiver is tuned.

Table 3-1. Operating Control and Indicators - Continued.

FIG. 3-1 INDEX NO.	NAME	REF. DES.	FUNCTION
2	BAND-MHZ control	A1S1 A2S1 A4S1 A5S1 A6S1 A7S1 A8S1	Selects one of five frequency bands as follows: 1.5-2.7 (Band 1) 1.5-2.7 MHz 2.7-5 (Band 2) 2.7 to 5 MHz 5-9 (Band 3) 5 to 9 MHz 9-17 (Band 4) 9 to 17 MHz 17-32 (Band 5) 17 to 32 MHz
3	ANTENNA TRIM control	C1	When not in the OFF position, it permits matching of receiver to antennas connected at WHIP ANT (J3) connector.
	Note: – When an antenna is connected to the LOW IMPD ANT (J2) connector the ANTENNA TRIM control must be in the OFF position because of its loading effect on the LOW IMPD ANT input connection.		
4	FINE TUNE control	R3	Vernier tuning control Provides tuning of the range -100 to +100 Hz about the frequency tuned by the TUNE control.
5	BFO KHZ control	C2	Controls frequency of BFO when DETECTOR switch is in CW.
6	DIV TUNE-ANT DSBL switch	S4	With a jumper between TB1-1 and TB1-2, the receiver operates normally in the OFF position. The antenna input circuits and RF amplifier A3 are disabled in the ON position. With the jumper removed, and the switch in the ON position, the antenna may be disabled by shorting TB1-1 and TB1-2 together. When the receiver is conditioned for diversity the local oscillator and counter are disabled in the ON and OFF positions, and turn-on in the DIV TUNE position (momentary contact).

Table 3-1. – Operating Control and Indicators - Continued.

FIG. 3-1 INDEX NO.	NAME	REF. DES.	FUNCTION
7	CARRIER-DB and LINE LEVEL DB meter	M1	Dual-scale indicator with one scale displaying line signal levels (audio output) and the other displaying carrier signal levels (rf signal output).
Note: – The position of the ISB MONITOR switch (index no. 22) determines which line channel is monitored when the DETECTOR switch is in one of the ISB positions.			
8	CARRIER-OFF-LINE switch	S5	Three-position switch used to select line or carrier levels at CARRIER and LINE LEVEL DB meter M1.
9	NAR-WIDE switch	A17S1	Controls bandwidth of audio circuit output connected to the PHONES jack J7 on front panel and the PHONE AUDIO OUT terminal TB1-8 on rear panel.
10	AUDIO GAIN control	A17R1	Adjusts audio level at the PHONES jack J7 on front panel and at the PHONE AUDIO OUT terminal TB1-8 on the rear panel.
11	LINE GAIN CH B control	R2B	Adjusts line audio output for the ISB channel B at TB1-6, -7 on the rear panel.
12	LINE GAIN CH A control	R2A	Adjusts line audio output for the main channel A at TB1-4, -5 on the rear panel.
13	RF GAIN control	R5	Allows manual control of receiver RF gain. Sets maximum RF gain with receiver in AGC.
14	LOCK-UNLOCK control	A21S1	Manually locks TUNE control when control is rotated counterclockwise to the LOCK position. Releases TUNE control for tuning when rotated to the UNLOCK position.
15	TUNE (coarse) control	A21C1	Coarse frequency control of receiver in all five RF bands.

Table 3-1. – Operating Controls and Indicators - Continued.

FIG. 3-1 INDEX NO.	NAME	REF. DES.	FUNCTION
16	TUNE (fine) control	A21C1	Fine frequency control of receiver in all five RF bands
17	DETECTOR switch	S3	Selects reception mode.
	AM/BFO		Amplitude-modulated signal reception with crystal BFO signal injected in receiver. Used primarily as a tuning aid and for accurate frequency measurement.
	AM		Amplitude-modulated signal reception.
	CW		Continuous-wave signal reception
	LSB		Lower sideband signal reception
	USB		Upper sideband signal reception
	ISB 3 KHZ		Independent sideband signal reception using 6 kHz bandwidth IF filter in conjunction with the USB and LSB filters.
	ISB 6 KHZ		Independent sideband signal reception using 16 kHz bandwidth IF filter in conjunction with the USB and LSB filters.
	FM		Frequency modulated signal reception
18	NOISE LIMITER control	A20R1	Controls amount of noise limiting applied to receiver audio output.
19	IF BANDWIDTH	A20S1	Controls bandwidth of IF amplifiers 0.1, 1, 2, 6, and 16 kHz bandwidths.

Table 3-1. – Operating Controls and Indicators - Continued.

FIG. 3-1 INDEX NO.	NAME	REF. DES.	FUNCTION
20	FUNCTION switch	S1	
	OFF		Removes all input power from receiver circuits.
	STBY		Receiver inoperative but available for instant use. Disconnects antenna input circuits and removes power from RF amplifier.
	AGC S		Slow-decay AGC response. Receiver gain controlled by strength of signal input.
	AGC M		Medium-decay AGC response. Receiver gain controlled by strength of signal input.
	AGC F		Fast-decay AGC response. Receiver gain controlled by strength of input signal.
	MGC		Turns off AGC and allows receiver RF gain to be controlled entirely by RF GAIN control
	SQUELCH		Silences receiver noise during periods when no signal is being received and sets gain control mode to AGC-M.
21	PHONES jack	J7	Front panel jack for monitoring of audio output by headphone.
22	ISB MONITOR switch	S2	Selects the ISB channel to be monitored when the DETECTOR switch is in the ISB 3 KHZ or ISB 6 KHZ position. When the DETECTOR switch is in any position except the two ISB positions the main channel audio may be monitored at the PHONES jack and at PHONE AUDIO OUT terminal TB1-8 on the rear panel via the audio bandwidth NAR-WIDE switch, when ISB MONITOR switch is in either CH A or CH B

Table 3-1. – Operating Controls and Indicators - Continued.

FIG. 3-1 INDEX NO.	NAME	REF. DES.	FUNCTION
			positions. The main channel line audio may also be monitored at the CARRIER-LINE LEVEL DB meter M1 when the CARRIER-OFF-LINE switch is in the LINE position.
	CH A		Connects the ISB channel A audio output to the PHONES jack and PHONE AUDIO OUT terminal TB1-8 on the rear panel via the audio bandwidth NAR-WIDE switch when the DETECTOR switch is in ISB 3 KHZ or ISB 6 KHZ. Also connects the ISB channel A line audio output to the CARRIER-LINE LEVEL meter M1 when the DETECTOR switch is in ISB 3 KHZ or ISB 6 KHZ, and when the CARRIER-OFF-LINE switch is in LINE.
	CH B		Same as for CH A except that the ISB channel B audio is monitored.

3-3. STARTING PROCEDURE. - Before operating the receiver, perform the following preliminary steps:

1. Energize external auxiliary equipment which will be used in conjunction with the receiver.

2. Set LOCK-UNLOCK control to UNLOCK.

3. Adjust RF GAIN control to MAX position.

4. Adjust FINE TUNE control to 0, mid-position.

5. Set DIV TUNE-ANT DSBL switch to OFF.

6. Set FUNCTION switch to AGC M.

7. Set audio NAR-WIDE switch to WIDE.

8. Set CARRIER-OFF-LINE switch to CARRIER.

9. Turn NOISE LIMITER control counterclockwise to the OFF position.

3-4. NORMAL OPERATING PROCEDURES. - The receiver may be used to receive AM, CW, SSB, ISB, FSK, and FM signals. Refer to table 1-1 in chapter 1 for a listing of the emission types. The reception of each type of signal requires the use of procedures unique to that type of signal. Special procedures must also be used for diversity operation or for reception of jammed signals.

a. AM Signal Reception. - AM signal reception may be accomplished as follows:

(1) Set the DETECTOR switch to the AM position.

(2) Set the IF BANDWIDTH switch to the 16 kHz position.

(3) Set the BAND-MHZ switch to the required frequency band.

(4) Set RF gain to MAX.

(5) Set FUNCTION switch to AGC-S.

(6) Using the TUNE control, tune the receiver to the desired signal. Adjust the TUNE control slightly to the left or right of the desired signal for a maximum CARRIER-DB meter indication. (Use the inner knob of the concentric TUNE control for rapid adjustment; use the outer knob for fine-frequency control.) The frequency readout may fluctuate randomly from the desired value to the next higher or lower value, but this effect is normal.

(7) Set ANTENNA TRIM control to OFF when the LOW IMPD ANT input is used. Adjust the ANTENNA TRIM control for maximum indication on CARRIER-DB meter when the WHIP ANT input is used.

(8) Adjust the LOCK-UNLOCK control to LOCK.

(9) Adjust the AUDIO GAIN control for a comfortable volume level.

(10) If there is excessive noise, adjust the NOISE LIMITER control clockwise as needed.

(11) If the signal fades rapidly, set the FUNCTION switch to AGC-M or AGC-F.

(12) If another station is interfering, set the IF BANDWIDTH switch to 6 kHz or 2 kHz.

(13) If receiver quieting is required between signal transmissions, set the FUNCTION switch to SQUELCH. (Gain control mode is then AGC-M.)

b. CW Signal Reception. - CW signal reception may be accomplished as follows:

(1) Set the DETECTOR switch to the CW position.

(2) Set the IF BANDWIDTH switch to the 2 kHz position.

(3) Set the BAND-MHZ switch to the required frequency band.

(4) Adjust the BFO KHZ control to 0, mid-position.

(5) Using the TUNE control, tune the receiver to zero beat with the desired signal. (Use the inner knob of the concentric TUNE control for rapid adjustment; use the outer knob for fine-frequency control.) The frequency readout may fluctuate randomly from the desired value to the next higher or lower value, but this effect is normal.

(6) Adjust the BFO KHZ control for a comfortable tone, or until any auxiliary equipment functions properly.

(7) Set ANTENNA TRIM control to OFF when the LOW IMPD ANT input is used. Adjust the ANTENNA TRIM control for maximum indication on CARRIER-DB meter when the WHIP ANT input is used.

(8) Adjust the LOCK UNLOCK control to LOCK.

(9) Adjust the AUDIO GAIN control for a comfortable volume level.

(10) If the keying of the signal is slow-speed, then set the FUNCTION switch to AGC-S, otherwise set it to MGC. Noise between keyed characters can be reduced by turning the RF GAIN control counterclockwise or by setting the FUNCTION switch to MGC, and reducing RF GAIN control to prevent blocking.

(11) If another station is interfering, then set the IF BANDWIDTH switch to 1 kHz, or if necessary to 0.1 kHz. Set audio switch to NAR.

c. SSB Signal Reception. - USB and LSB signal reception may be accomplished as follows:

(1) Set the DETECTOR switch to the USB or LSB position, whichever is appropriate for the signal being received.

(2) Set FUNCTION switch to AGC-S.

(3) Set the BAND-MHZ switch to the required frequency band.

(4) Using the TUNE control, tune the receiver to the desired signal. Adjust the TUNE control slightly to the left or right of the desired signal until the intelligence of the signal becomes clear. (Use the inner knob of the concentric TUNE control for rapid adjustment; use the outer knob for fine-frequency control.) If necessary, adjust the FINE TUNE control until the signal becomes clear. The frequency readout may fluctuate randomly from the desired value to the next higher or lower value, but this effect is normal.

(5) Set ANTENNA TRIM control to OFF when the LOW IMPD ANT input is used. Adjust the ANTENNA TRIM control for maximum indication on CARRIER-DB meter when the WHIP ANT input is used.

(6) Adjust the LOCK UNLOCK control to LOCK.

(7) Adjust the AUDIO GAIN control for a comfortable volume level.

(8) Set the FUNCTION switch to AGC-S or AGC-M depending on the fading rate.

d. ISB Signal Reception. - ISB signal reception may be accomplished as follows:

(1) Set the DETECTOR switch to either ISB 3 KHZ or ISB 6 KHZ, depending on auxiliary-equipment frequency requirements and available bandwidth in the frequency spectrum.

(2) Set FUNCTION switch to AGC-S.

(3) Set the BAND-MHZ switch to the required frequency band.

(4) Using the TUNE control, tune the receiver to the desired signal. Adjust TUNE control slightly to the left or right of the desired signal until the intelligence of the signal becomes clear. (Use the inner knob of the concentric TUNE control for rapid adjustment; use the outer knob for fine-frequency control.) If necessary, adjust the FINE TUNE control until the signal becomes clear. The frequency readout may fluctuate randomly from the desired value to the next higher or lower value, but this effect is normal.

(5) Set ANTENNA TRIM control to OFF when the LOW IMPD ANT input is used. Adjust the ANTENNA TRIM control for maximum indication on CARRIER-DB meter when the WHIP ANT input is used.

(6) Adjust the LOCK UNLOCK control to LOCK.

(7) Adjust the AUDIO GAIN control for a comfortable volume level. Either channel may be monitored by setting the ISB MONITOR switch in the appropriate position.

(8) Set the FUNCTION switch to AGC-S or AGC-M depending on the fading rate.

e. FM Signal Reception. - FM signal reception may be accomplished as follows:

(1) Set the DETECTOR switch to FM.

(2) Set the IF BANDWIDTH switch to 16 kHz.

(3) Set FUNCTION switch to AGC-S.

(4) Set the BAND-MHZ switch to the required frequency band.

(5) Using the TUNE control, tune the receiver to the desired signal. First tune for a maximum indication on the CARRIER-DB meter, then adjust the TUNE control slightly to the left or right of the desired signal until the intelligence of the signal becomes clear. (Use the inner knob of the concentric TUNE control for rapid adjustment; use the outer knob for fine-frequency control.) If necessary, adjust the FINE TUNE control until the signal becomes clear. The frequency readout may fluctuate randomly from the desired value to the next higher or lower value, but this effect is normal.

(6) Set ANTENNA TRIM control to OFF when the LOW IMPD ANT input is used. Adjust the ANTENNA TRIM control for maximum indication on CARRIER-DB meter when the WHIP ANT input is used.

(7) If interference exists on the signal (either from other stations or from atmospheric noise), then decrease the IF BANDWIDTH to 6 kHz, 2 kHz, or as narrow as neccessary for reliable reception. However, do not decrease the bandwidth so low as to prevent the signal from being received at all.

(8) Adjust the LOCK-UNLOCK control to LOCK.

(9) If noise is still present on the signal, then increase the NOISE LIMITER control as far as necessary.

(10) If the signal fades, set the FUNCTION switch to AGC F.

(11) Adjust the AUDIO GAIN control for a comfortable volume level.

(12) If receiver quieting is required between signal transmissions, then set the FUNCTION switch to SQUELCH.

f. Frequency-Shift Keying Signal Reception. - Frequency-shift signal reception may be accomplished as follows:

(1) Set the DETECTOR switch to the CW position.

(2) Set the IF BANDWIDTH switch to the 2 kHz position.

(3) Set FUNCTION switch to AGC-S.

Note: – If a wide-shift FSK signal is being received, use the optional 3.5 kHz (FL21) in place of the 2 kHz (FL4) filter.

(4) Set the BAND-MHZ switch to the required frequency band.

(5) Adjust the BFO KHZ control to 0, mid-position.

(6) Set audio bandwidth NAR-WIDE switch to WIDE.

(7) Using the TUNE control, tune the receiver to the desired signal, then readjust slightly until mark and space signals with the same tone are heard.

(8) Set the CARRIER-OFF-LINE switch to LINE.

(9) Adjust the CH A LINE GAIN control for +3 db indication on the LINE LEVEL DB meter.

(10) Adjust the BFO KHZ control to ±5.5 kHz and fine tune until mark and space lines are of equal length and intensity when displayed on the demodulator display.

g. Diversity Operation. - Diversity reception minimizes the effect of fading signals and provides substantially uniform audio output. Each of two receivers are connected to a different antenna. The local oscillator output of a master receiver (the receiver conditioned for normal operation) is connected to a slave receiver (the receiver conditioned for diversity operation). The AGC circuits of both receivers are connected together so that the receiver receiving the strongest signal controls the gain of the other receiver. The audio outputs of both receivers are connected in parallel. Once the receivers have been connected for diversity reception (refer to chapter 2 for setup instructions), the operation is as follows:

(1) Adjust the RF GAIN control of the slave receiver (the NORMAL-DIVERSITY switch A16S1 (see figure 1-3) is set to DIVERSITY) counterclockwise to 0.

(2) Tune in the desired signal on the master receiver (the NORMAL-DIVERSITY switch on A16 is set to NORMAL) using the operating procedures discussed in paragraphs 3-4a through e.

(3) Adjust the RF GAIN on the master receiver to 0.

(4) Adjust the RF GAIN on the slave receiver to MAX.

(5) Tune in the same signal on the slave receiver by holding the DIV TUNE-ANT DSBL switch in the DIV TUNE position using the same operating procedure as for the master receiver. Once the slave receiver is tune to the same signal as the master receiver, release the DIV TUNE-ANT DSBL switch. This extinguishes the FREQUENCY MHZ display on the slave receiver.

(6) Adjust the RF GAIN control on the master receiver to MAX. The receivers are now tuned to the same signal, and they are operating as a diversity system.

(7) If it becomes necessary to change frequencies, repeat steps (1) through (6).

h. Antijamming Instructions. - When receiving jammed signals, follow the procedures in the order indicated below until the signal is heard with the least amount of interference.

(1) Adjust the TUNE control and the FINE TUNE control very slowly to either side of the desired signal. Some separation of the desired signal from the jamming signal may be achieved.

(2) If receiving AM, CW, or FM, then set the IF BANDWIDTH switch to a narrower bandwidth, and try tuning again as described in (1).

(3) If the WHIP ANT input is used, adjust the ANTENNA TRIM control to the point where the signal is heard with the least amount of interference.

(4) If the noise is severe, adjust the NOISE LIMITER control as required.

(5) When the jamming signal is weak, turn the FUNCTION switch to MGC and the RF GAIN control counterclockwise. The interfering signal may be reduced enough to permit the desired signal to come through.

(6) Set the audio switch to NAR.

(7) If possible, change the direction, length, and height of the antenna. This may reduce the jamming effectiveness so that some degree of satisfactory reception is obtained.

3-5. STOPPING PROCEDURE.

a. When the receiver is not to be used but is to be maintained in a state of readiness, turn the FUNCTION switch to STBY.

b. To shut the receiver off, turn the FUNCTION switch to OFF.

CHAPTER 4

PRINCIPLES OF OPERATION

4-1. GENERAL. - This chapter provides an overall functional description of the receiver and the functional description of each major assembly.

4-2. OVERALL BLOCK DIAGRAM DESCRIPTION. - See figure 4-1 for a block diagram and figure A-28 for a schematic diagram of the HF General Purpose Radio Receiver R-1414/URR.

a. RF Section. - The RF section is divided into five bands and the main tuning (TUNE control) is accomplished by use of a gear-driven, five-section, air-variable capacitor. Refer to table 4-1 for a listing of the RF input limits, first local oscillator frequency limits, and the first IF frequencies for each frequency band. Four capacitor sections tune the RF filters on boards A1, A2, A4, and A5. The fifth section tunes the first local oscillator A7. The RF band switch (BAND-MHZ switch) is a detented, gear-driven, front panel switch for use in selection of the frequency band of interest. The actual electrical switching takes place on the A1, A2, A4, A5, A6, A7, and A8 boards by use of four section-five position switches which are mounted on the above-mentioned printed circuit boards. The individual wafers are ganged together and coupled to the front-panel control.

(1) RF signals from an antenna coaxial transmission line are coupled into the receiver at the rear panel through the LOW IMPD ANT connector J2 (C type). The input signals from J2 are coupled through RFI filter FL19 which reduces harmonic radiations from the first local oscillator. The signals are then passed through the antenna disabling relay A1K1, through sections of the BAND-MHZ switch, through an overload protection circuit to the first RF double-tuned selective filter (boards A1 and A2). When a whip antenna is used,the RF signals enter the receiver through the WHIP ANT connector J3 (BNC type), through the antenna disabling relay A1K1, through sections of the BAND-MHZ switch to the whip antenna tuning circuit which is part of the ANTENNA TRIM circuit. A different coil is used for each band and the circuit is tuned by the antenna trimmer capacitor to provide maximum coupling into the first RF double-tuned selective filter (boards A1 and A2). The ANTENNA TRIM control disables the whip antenna input when it is in the OFF position. This generally provides the optimum coupling for the LOW IMPD ANT input, however, in some instances adjustment of the ANTENNA TRIM control may improve sensitivity. The antenna disabling relay, which is front panel controlled by the DIV TUNE-ANT DSBL switch S4 or by the STBY position of FUNCTION switch S1, is used to allow operation of the receiver with a transmitter connected to the same antenna and also disables the receiver during standby operation. The proper double-tuned filter is selected by the position of the BAND-MHZ switch. The S1B portions of the BAND-MHZ switch on boards A1, A2, A4, and A5 are used to short the circuits that are not used. These are shown on the schematic diagrams but are not shown on the block diagram for clarity. The antenna trimmer circuit consists of front panel control ANTENNA TRIM C1 and coils A1L21 through A1L25. The neon lamp DS1 prevents large input signals from damaging the input circuits of the receiver. The first double-tuned filter provides selectivity to eliminate undesired frequencies and is comprised of components on

antenna tuner A1 and RF tuner A2 plus two sections of the air-variable tuning capacitor A21C1 as shown in figure 4-2.

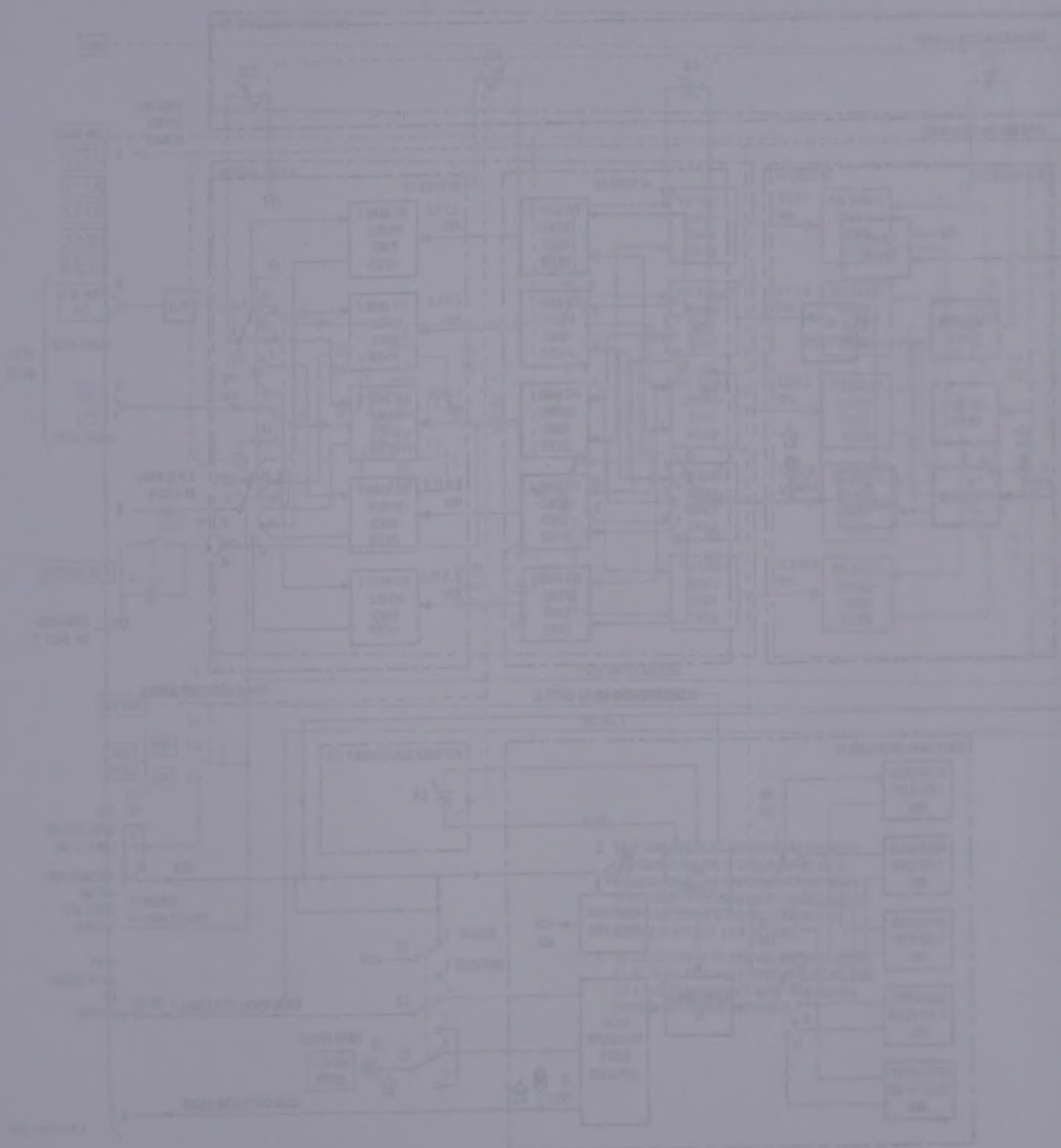
(2) The desired signal next enters the RF amplifier board A3. Depending on signal level, this circuit provides various amounts of gain in accordance with the AGC level fed back from the level-detecting AGC circuits in the IF section of the receiver. Protection diodes are connected to the input of the two RF amplifiers to protect the amplifier against high input signal levels. The amplifiers can be completely turned-off by the 25-volt switch that is controlled by the same two switches (DIV TUNE-ANT DSBL switch S4 and FUNCTION switch S1) that control the antenna disable relay A1K1.

(3) The RF output of amplifier A3 is coupled to the input of the second double-tuned filter on RF tuner A4. Components on RF tuners A4 and A5 comprise the second double-tuned filters and provide further selectivity to eliminate undesired frequencies.

(4) The RF signal from RF tuner A5 is then converted to one of three, first intermediate frequencies in the first mixer board A6. The RF signal and the local oscillator signal from the RF local oscillator A7 are mixed in a double-balanced mixer. Depending on the band being used, the intermediate frequencies are generated as shown in table 4-1. The intermediate frequencies are coupled to one of the corresponding IF crystal filters FL1 through FL3 by the BAND-MHZ switch via IF transformers A6T3 through A6T5. The outputs of the crystal filters are next applied to the first IF amplifier A10.

(5) The RF local oscillator A7 is a modified Hartley design. Five oscillator circuits generate the local oscillator frequencies required to develop the required intermediate frequencies. The oscillators are tuned for frequencies that are higher than the input RF signal by the first intermediate frequencies. The required oscillator is selected by the BAND-MHZ switch which is ganged to switch S1 on board A7. All oscillator circuits are tuned by section CIE of the main tuning capacitor. A varactor diode is installed across section CIE of the tuning capacitor and is controlled by the AFC voltage received from AFC board A8. The RF local oscillator A7 provides three outputs. One output is coupled to the LOC OSC IN/OUT connector J4 on the rear panel when the NORMAL-DIVERSITY switch A16S1 is in the NORMAL position. A second output is also coupled through the NORMAL position of A16S1 to the first mixer A6. When switch A16S1 is in the NORMAL position a third set of switch contacts connects +25 vdc (B+ voltage) to the +25 volt regulator in the RF local oscillator A7 and to counter A9. When switch A16S1 is in the DIVERSITY position a local oscillator signal may be connected from the LOC OSC IN/OUT connector J4 on the rear panel to the first mixer A6. The RF local oscillator A7 and counter A9 may now be temporarily turned-on to allow tuning of the receiver when the DIV TUNE-ANT DSBL switch S4 is pushed and held in the DIV TUNE position. A third output of RF local oscillator A7 bypasses switch A16S1 and is coupled directly to counter A9.

b. Counter and AFC. - The frequency counter A9 is used to count the frequency of the RF local oscillator. To provide direct readout of the frequency to which the receiver is tuned, the counter decades are preset to subtract the first intermediate frequency from the local oscillator frequency count. Six digits are displayed; the most-significant-digit represents tens of megahertz and the least-significant-digit represents hundreds of Hertz. A digital storage register, called memory, stores the information representing the desired least-significant-digit. At the completion of each



antenna tuner A1 and RF tuner A2 plus two sections of the air-variable tuning capacitor A21C1 as shown in figure 4-2.

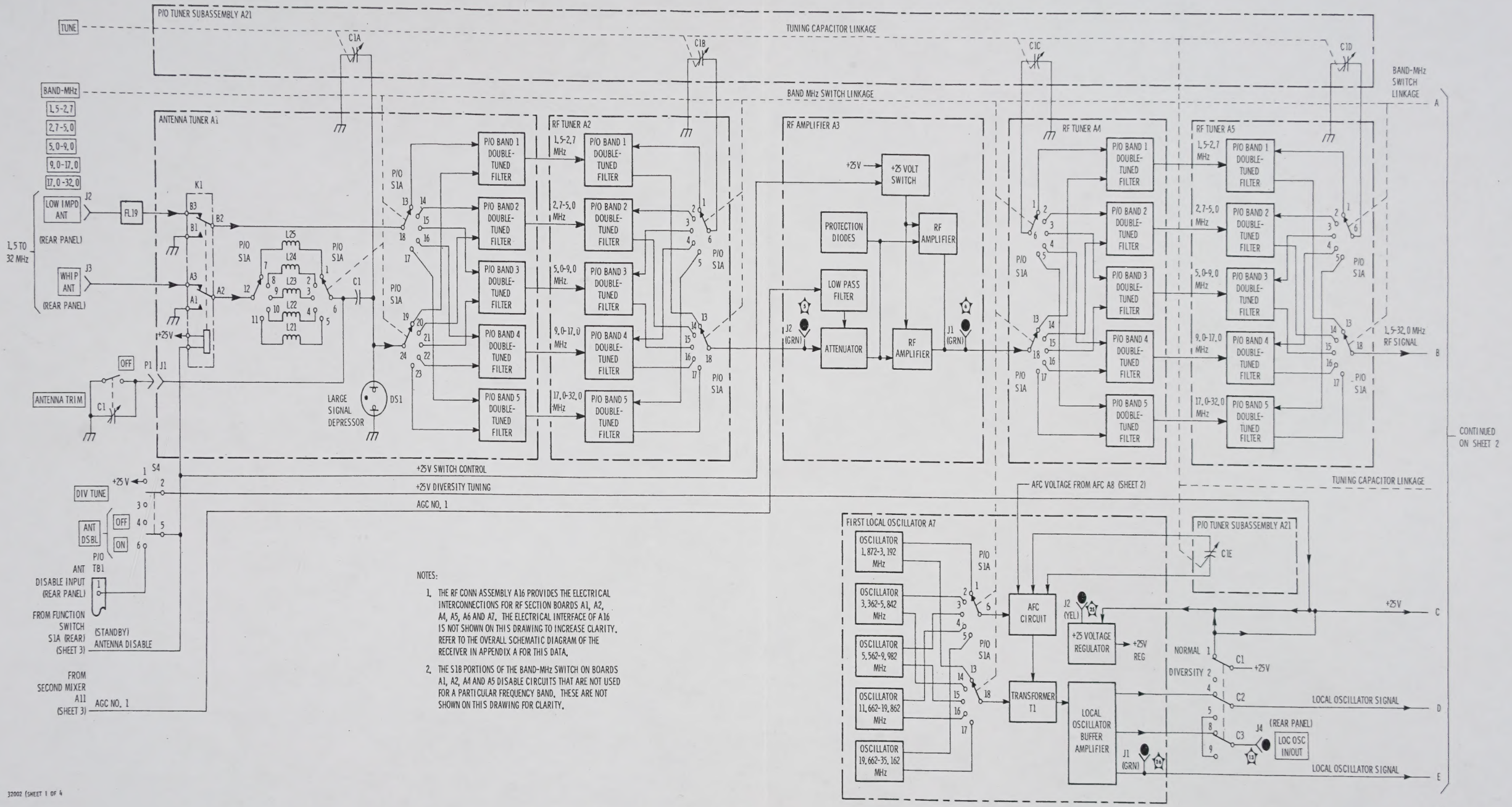
(2) The desired signal next enters the RF amplifier board A3. Depending on signal level, this circuit provides various amounts of gain in accordance with the AGC level fed back from the level-detecting AGC circuits in the IF section of the receiver. Protection diodes are connected to the input of the two RF amplifiers to protect the amplifier against high input signal levels. The amplifiers can be completely turned-off by the 25-volt switch that is controlled by the same two switches (DIV TUNE-ANT DSBL switch S4 and FUNCTION switch S1) that control the antenna disable relay A1K1.

(3) The RF output of amplifier A3 is coupled to the input of the second double-tuned filter on RF tuner A4. Components on RF tuners A4 and A5 comprise the second double-tuned filters and provide further selectivity to eliminate undesired frequencies.

(4) The RF signal from RF tuner A5 is then converted to one of three, first intermediate frequencies in the first mixer board A6. The RF signal and the local oscillator signal from the RF local oscillator A7 are mixed in a double-balanced mixer. Depending on the band being used, the intermediate frequencies are generated as shown in table 4-1. The intermediate frequencies are coupled to one of the corresponding IF crystal filters FL1 through FL3 by the BAND-MHZ switch via IF transformers A6T3 through A6T5. The outputs of the crystal filters are next applied to the first IF amplifier A10.

(5) The RF local oscillator A7 is a modified Hartley design. Five oscillator circuits generate the local oscillator frequencies required to develop the required intermediate frequencies. The oscillators are tuned for frequencies that are higher than the input RF signal by the first intermediate frequencies. The required oscillator is selected by the BAND-MHZ switch which is ganged to switch S1 on board A7. All oscillator circuits are tuned by section CIE of the main tuning capacitor. A varactor diode is installed across section CIE of the tuning capacitor and is controlled by the AFC voltage received from AFC board A8. The RF local oscillator A7 provides three outputs. One output is coupled to the LOC OSC IN/OUT connector J4 on the rear panel when the NORMAL-DIVERSITY switch A16S1 is in the NORMAL position. A second output is also coupled through the NORMAL position of A16S1 to the first mixer A6. When switch A16S1 is in the NORMAL position a third set of switch contacts connects +25 vdc (B+ voltage) to the +25 volt regulator in the RF local oscillator A7 and to counter A9. When switch A16S1 is in the DIVERSITY position a local oscillator signal may be connected from the LOC OSC IN/OUT connector J4 on the rear panel to the first mixer A6. The RF local oscillator A7 and counter A9 may now be temporarily turned-on to allow tuning of the receiver when the DIV TUNE-ANT DSBL switch S4 is pushed and held in the DIV TUNE position. A third output of RF local oscillator A7 bypasses switch A16S1 and is coupled directly to counter A9.

b. Counter and AFC. - The frequency counter A9 is used to count the frequency of the RF local oscillator. To provide direct readout of the frequency to which the receiver is tuned, the counter decades are preset to subtract the first intermediate frequency from the local oscillator frequency count. Six digits are displayed; the most-significant-digit represents tens of megahertz and the least-significant-digit represents hundreds of Hertz. A digital storage register, called memory, stores the information representing the desired least-significant-digit. At the completion of each

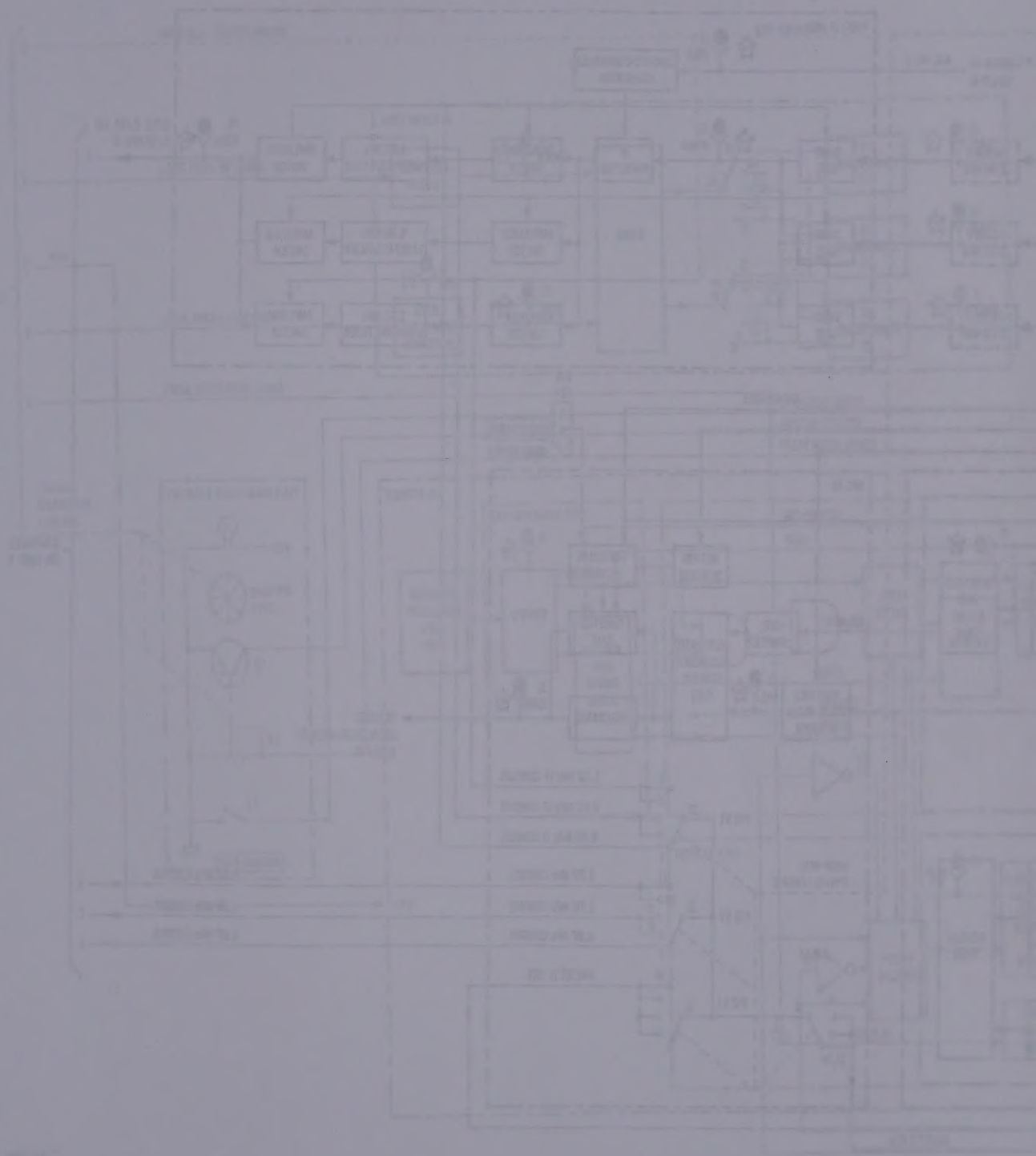


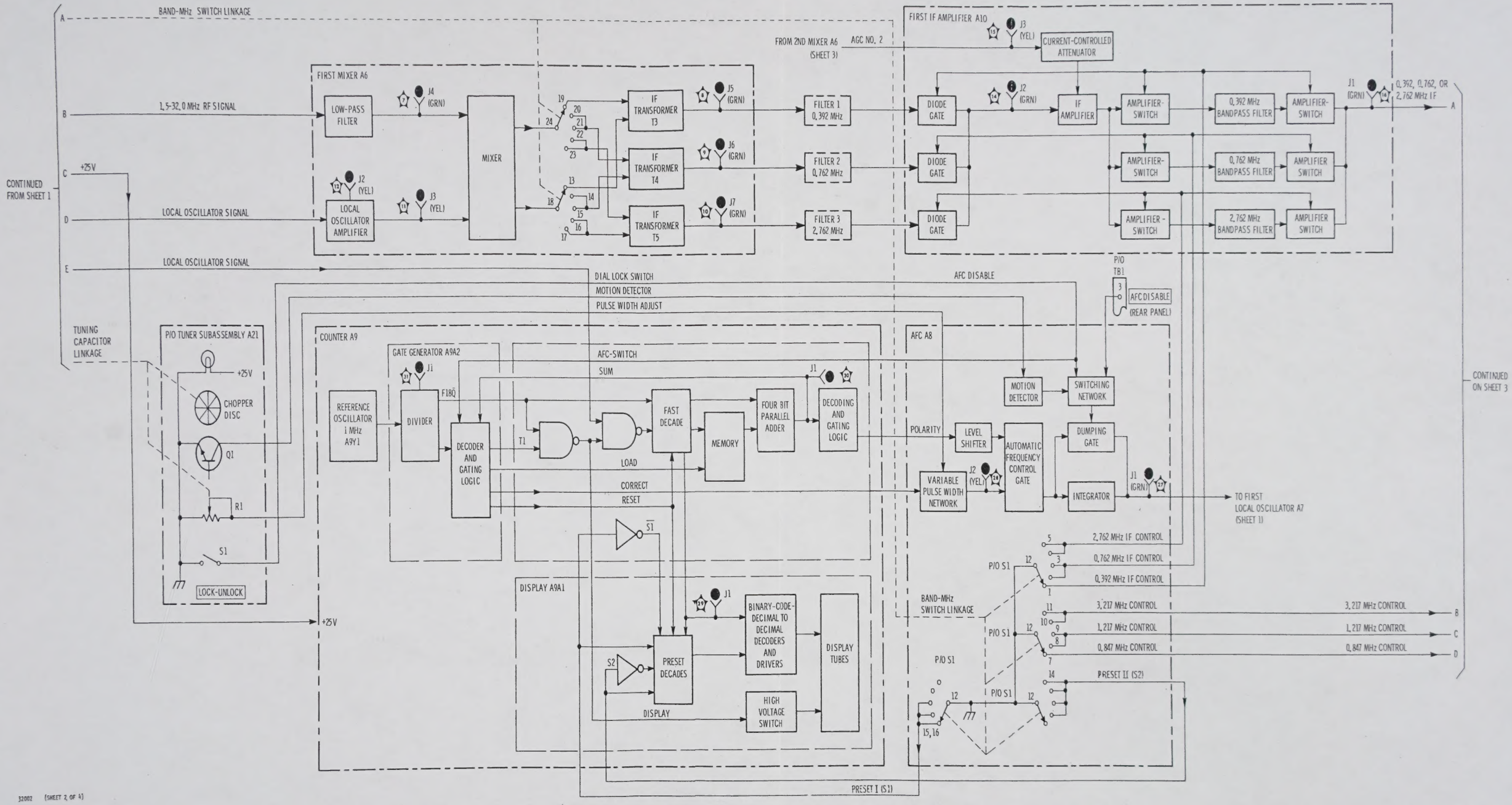
NOTES:

1. THE RF CONN ASSEMBLY A16 PROVIDES THE ELECTRICAL INTERCONNECTIONS FOR RF SECTION BOARDS A1, A2, A4, A5, A6 AND A7. THE ELECTRICAL INTERFACE OF A16 IS NOT SHOWN ON THIS DRAWING TO INCREASE CLARITY. REFER TO THE OVERALL SCHEMATIC DIAGRAM OF THE RECEIVER IN APPENDIX A FOR THIS DATA.
2. THE S1B PORTIONS OF THE BAND-MHz SWITCH ON BOARDS A1, A2, A4 AND A5 DISABLE CIRCUITS THAT ARE NOT USED FOR A PARTICULAR FREQUENCY BAND. THESE ARE NOT SHOWN ON THIS DRAWING FOR CLARITY.

32002 (SHEET 1 OF 4

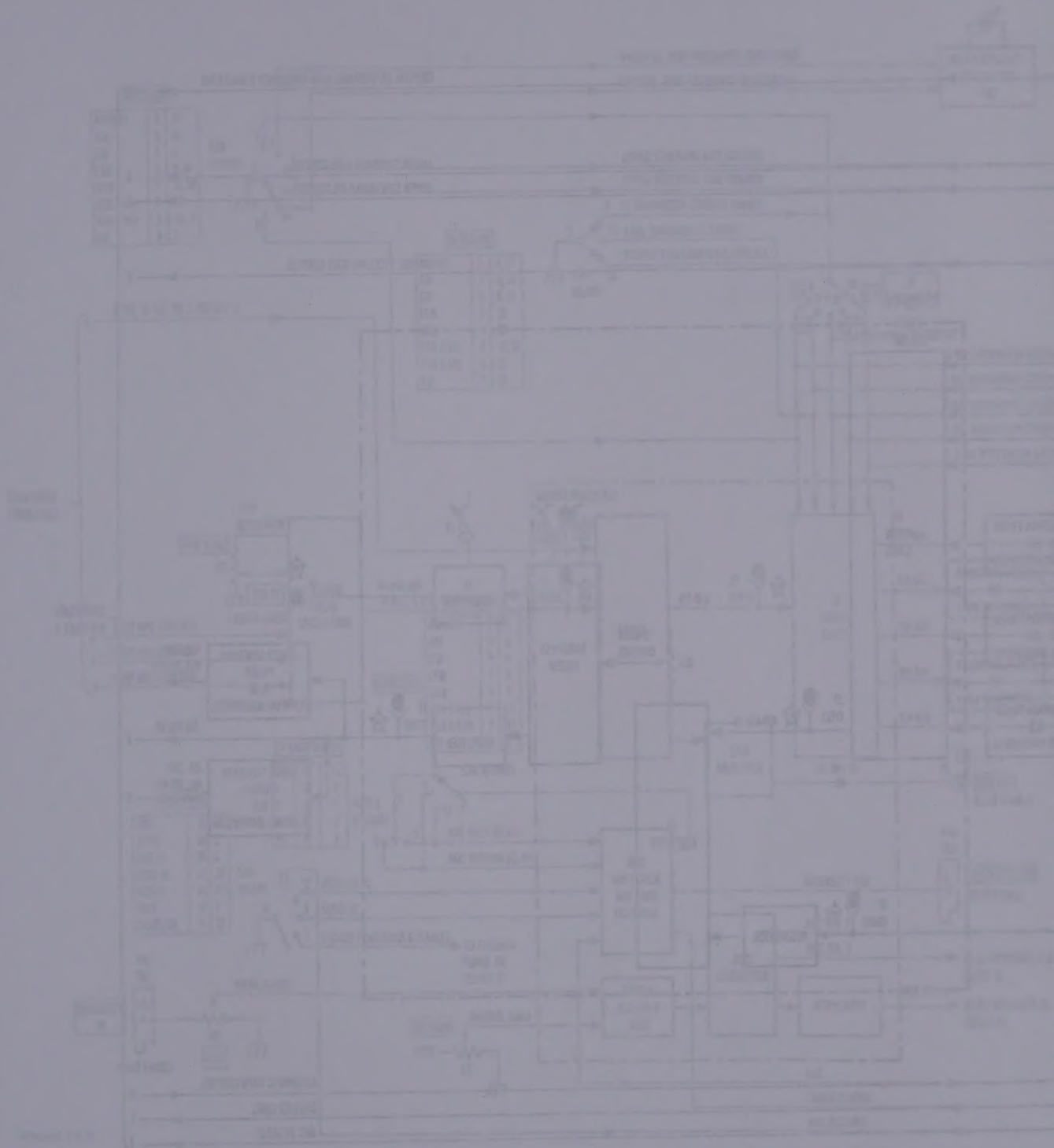
Figure 4-1. - HF General Purpose Radio Receiver R-1414/URR, Block Diagram (Sheet 1 of 4)





32002 (SHEET 2 OF 4)

Figure 4-1. - HF General Purpose Radio Receiver R-1414/URR, Block Diagram (Sheet 2 of 4)



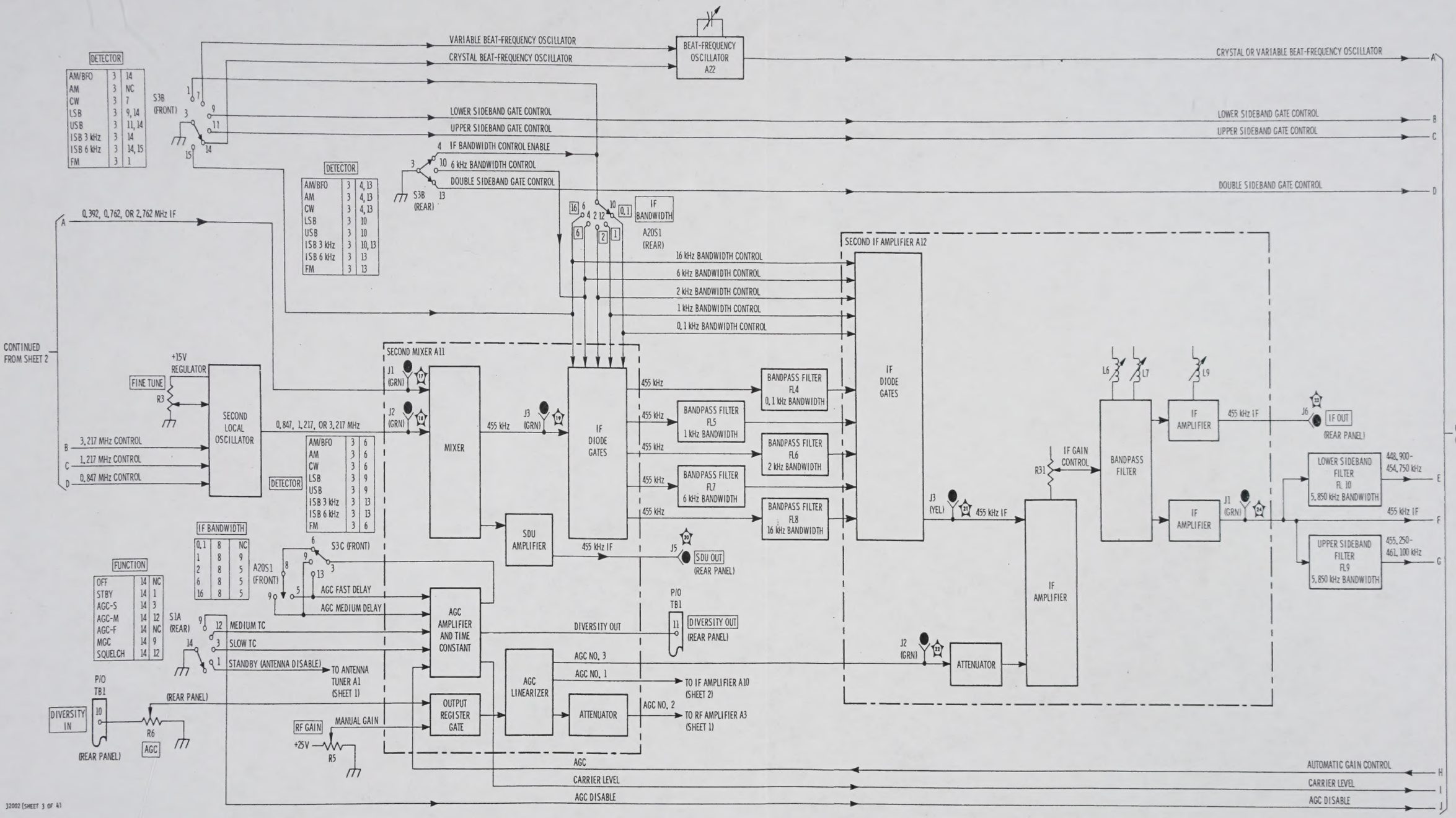
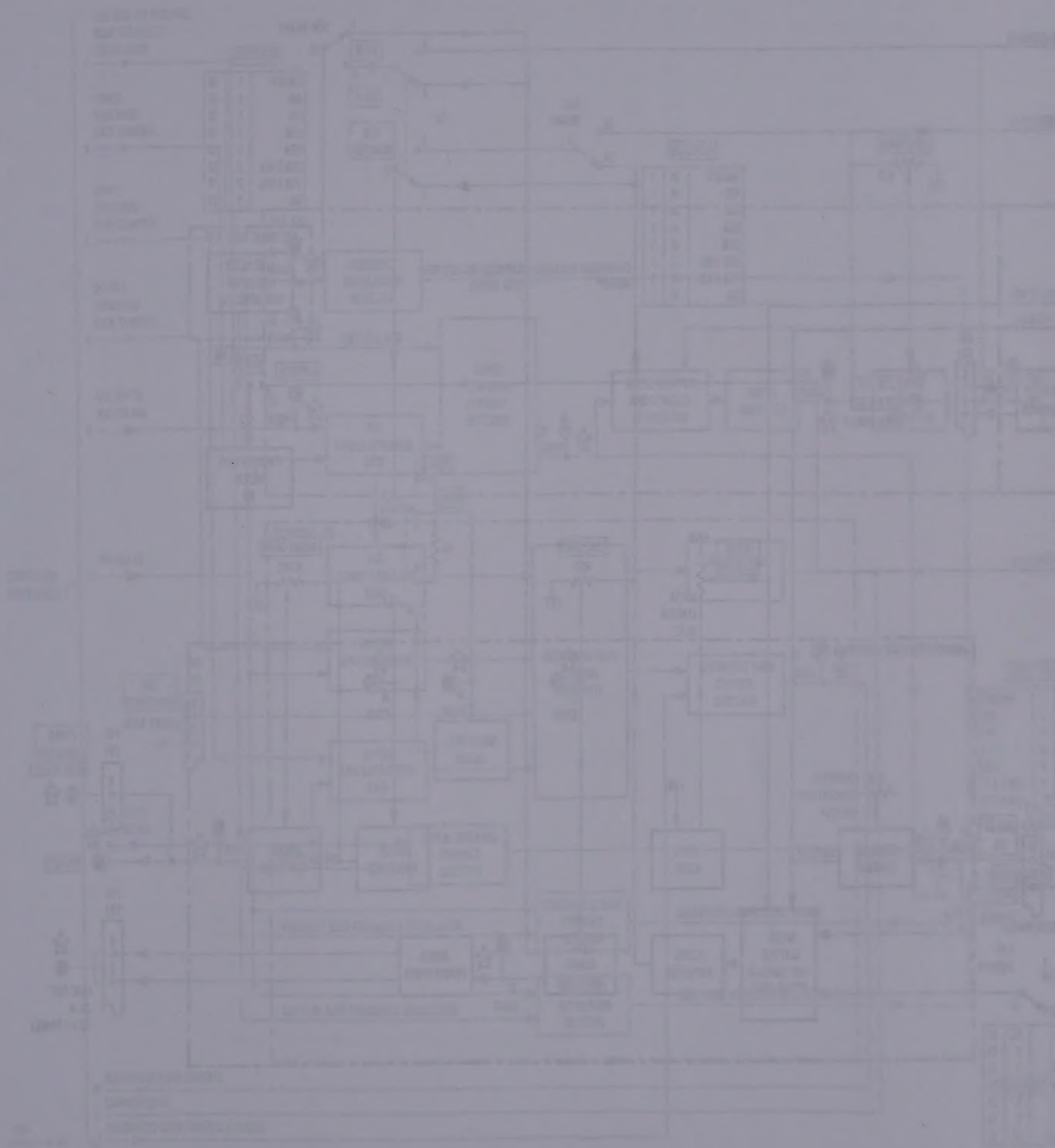


Figure 4-1. – HF General Purpose Radio Receiver R-1414/URR, Block Diagram (Sheet 3 of 4)



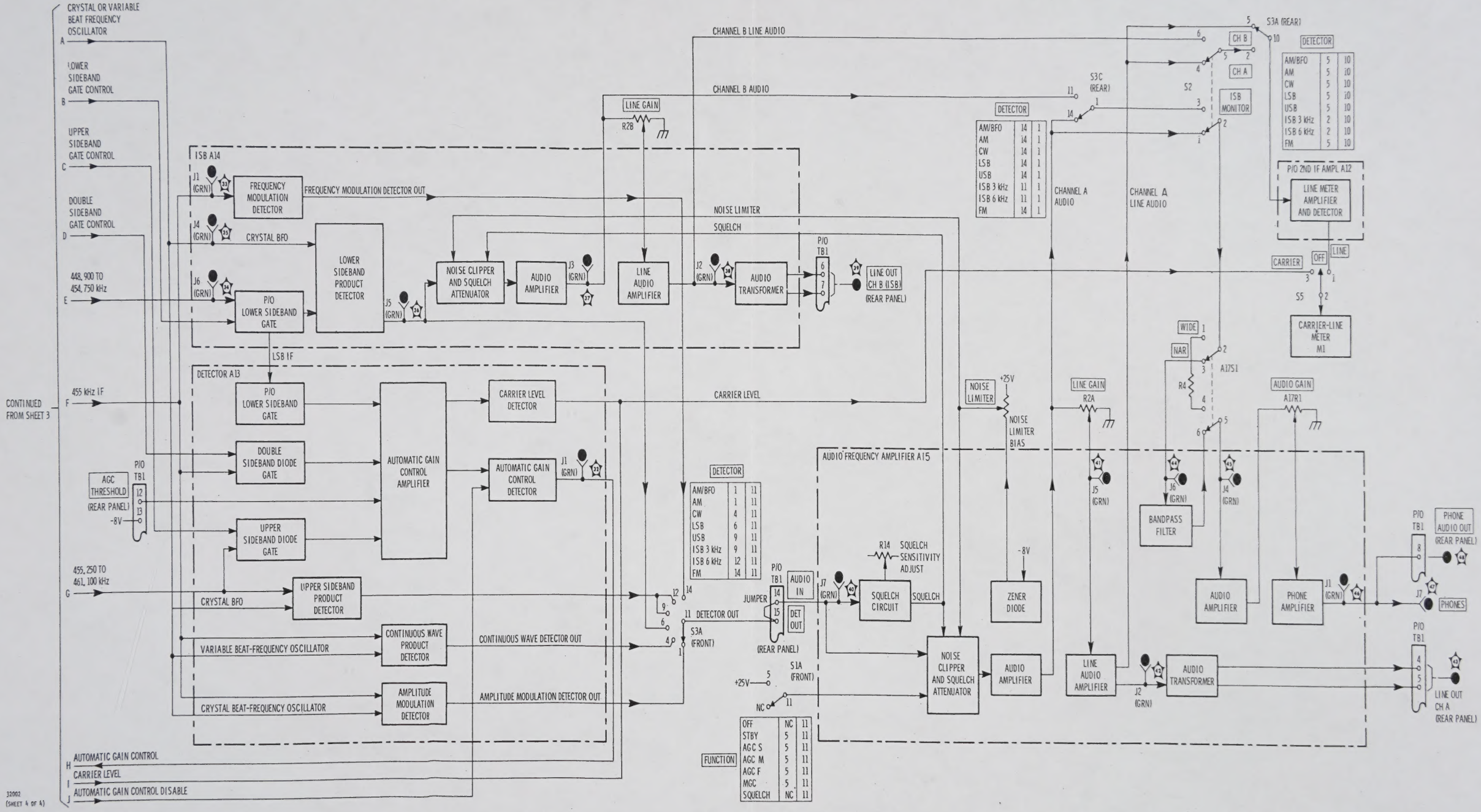


Figure 4-1. – HF General Purpose Radio Receiver R-1414/URR, Block Diagram (Sheet 4 of 4)

Table 4-1. – Input, LO, and First IF Frequencies.

BAND	RF FREQUENCY (MHz)	1ST LO FREQUENCY (MHz)	1ST IF FREQUENCY (MHz)
1 low	1.48	1.872	0.392
high	2.80	3.192	0.392
2 low	2.60	3.362	0.762
high	5.08	5.842	0.762
3 low	4.80	5.562	0.762
high	9.22	9.982	0.762
4 low	8.90	11.662	2.762
high	17.1	19.862	2.762
5 low	16.9	19.662	2.762
high	32.4	35.162	2.762

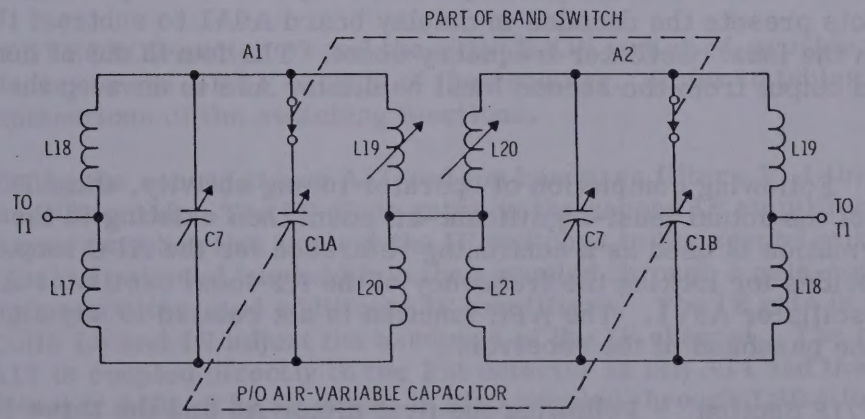


Figure 4-2. –Double-Tuned Filter

count period a comparison is made between the actual counted least-significant-digit and the stored information. If an error exists, a correction and polarity (depending on whether the oscillator frequency is high or low) pulses are coupled to the AFC board A8.

(1) The correction pulses are first coupled through a variable pulse width network in AFC board A8. The network also receives a Pulse Width Adjust input from a logarithmic-taper potentiometer A21A1 on the tuning shaft, since pulses of varying widths are needed in order to keep the amount of AFC frequency correction constant at about 3.5 Hz per correct pulse. The variable pulse width network enables the AFC gate to allow the level shifter output to drive the integrator. The level shifter provides an appropriate level output to drive the integrator depending upon the polarity input. The dc AFC voltage output of the integrator is applied to a varactor diode in the AFC circuit of the RF local oscillator at A7. This controls the frequency of the local oscillator when the receiver is not being tuned. When the receiver is being tuned, a phototransistor Q1 in tuner subassembly A21 sends a signal to the motion detector circuit. The switching network then closes the dumping gate. This turns the AFC function off. One other input to the switching network also causes the AFC function to be disabled. This is the input from TB1-3 (AFC DISABLE input) on the rear panel. If TB1-3 is grounded, the switching network disables the AFC function. The front panel LOCK UNLOCK switch A21S1 also applies a ground to the switching network when it is set to LOCK which locks the main TUNE control. This ground (AFC-SW) is also coupled to the decoder and gating logic in gate generator A9A2, which prevents a load output in cases of unintentional movement of the tuning control.

(2) A portion of the BAND-MHZ switch is also located on the AFC board A8. One set of switch A8S1 contacts (not shown on block diagram) connect different input resistances to the integrator to keep the frequency correction constant. A second set of switch A8S1 contacts selects the required IF input to IF amplifier A10. A third set of contacts presets the decades in display board A9A1 to subtract the first IF frequency from the local oscillator frequency count. The fourth set of contacts selects the required output from the second local oscillator A18 to develop the final IF of 455 kHz.

(3) Following completion of operator tuning activity, the AFC loop causes the storing of the actual least-significant-bit count then existing in the counter. That stored information is used as a continuing reference for the AFC loop. The AFC function provides for locking the frequency of the RF local oscillator A7 to the 1 MHz reference oscillator A9Y1. The AFC function is not related to any signal that may be present in the passband of the receiver.

c. AF/IF Section. - Following the first mixer A6 and the three IF filters FL1, FL2, and FL3 is the first IF Amplifier A10, which is gain-controlled by the AGC circuits on the second mixer board A11. At the input of the IF amplifier one of the three diode gates selects one of the three IF outputs depending on the frequency band selected by the BAND-MHZ switch, as detailed in table 4-1. This IF input is then coupled through a gain-controlled IF amplifier. The output of this IF amplifier is then switched through one of three IF channels, depending again upon the frequency band selected by the BAND-MHZ switch. After further amplification and filtering, one of the three first intermediate frequencies is then coupled to the second mixer A11.

(1) The second mixer is a conventional transistor mixer which mixes the signals from the first IF amplifier A10 and the second local oscillator A18 to obtain

the second IF of 455 kHz. The second local oscillator A18 is a crystal oscillator operating at 455 kHz above the first IF frequency. The FINE TUNE adjusts the second local oscillator frequency by ±100 Hz. The 455 kHz IF output of the mixer is coupled through IF diode gates to IF filters which provide the receivers selectivity. Five selectivity ranges are selectable from the front panel IF BANDWIDTH control: 0.1 kHz, 1.0 kHz, 2.0 kHz, 6.0 kHz, and 16.0 kHz. These are selectable when the front panel DETECTOR switch is in the AM/BFO, AM, CW, or FM positions. The 6 kHz bandwidth is selected directly by the DETECTOR switch when in the LSB, USB, or ISB 3 KHZ positions. The 16 kHz bandwidth is selected directly by the DETECTOR switch when in the ISB 6 KHZ position. Another 455 kHz IF output is available at SDU OUT connector J5 on the rear panel. This output has a constant bandwidth in excess of 16 kHz.

(2) The second mixer A11, together with the detector A13, also contains AGC circuits. As shown in figure 4-3, the AGC circuits consist of a detector amplifier, detector, amplifier, and linearizer. These circuits provide a dc voltage which is proportional to the IF signal level. The variable recovery time constants (the first part of the AGC decay time) are obtained by the three capacitors which are selected by positions AGC S, AGC M, and AGC F of the FUNCTION switch. The second part of the AGC decay time is controlled by the IF BANDWIDTH switch and the DETECTOR switch. When the FUNCTION switch is in the MGC position, the AGC circuits may be controlled manually by use of the RF GAIN control R5. The AGC circuits may also be controlled from another receiver when two receivers are connected for diversity operation. The AGC outputs are coupled to the second IF amplifier A12, first IF amplifier A10, and RF amplifier A3. An AGC Diversity output is also sent to the TB1-11 (DIVERSITY OUT) on the rear panel. A carrier-level output is sent to the CARRIER-LINE LEVEL DB meter M1 via the CARRIER-OFF-LINE switch S5. This output supplements the carrier level output from the detector A13 for high level signal inputs to the receiver.

(3) The DETECTOR switch S3 and the FUNCTION switch S1 provide most of the switching functions for the AF/IF section of the receiver. Refer to tables 4-2 and 4-3 for detailed explanations of the switching functions.

(4) Following the second mixer A11 and the bandpass filters FL4 through FL8 is the second IF amplifier A12. The IF diode gates in the second IF amplifier A12 are controlled by the same switches that control the IF switches in the second mixer A11. The 455 kHz IF signal of selected bandwidth is then coupled through a gain-controlled IF amplifier, a bandpass filter, and additional IF amplifiers. The IF gain is adjustable by R31 and L9. Coils L6 and L7 adjust the bandpass of the IF channel. The output of the IF amplifier A12 is coupled directly to the FM detector in ISB A14 and the AM and CW detectors in detector A13. The IF output is also coupled through LSB filter FL10 and USB filter FL9 to the LSB product detector in ISB A14 and USB product detector in detector A13. Another IF output is available at IF connector J6 on the rear panel.

(5) The detector board A13 contains the AM, CW, USB, and AGC detectors; the ISB board A14 contains the FM and LSB detectors. The LSB and USB product detectors are driven by a crystal-controlled BFO in BFO A22 when the DETECTOR switch is in the AM/BFO, LSB, USB, ISB 3 KHZ and ISB 6 KHZ positions. The CW detector is driven by a front panel controlled variable BFO in BFO A22 when the DETECTOR switch is in the CW position. The DETECTOR switch selects the detector outputs that are coupled to the DET OUT terminal TB1-15 on the rear panel. A jumper, normally installed between TB1-15 and TB1-14, couples the detector output

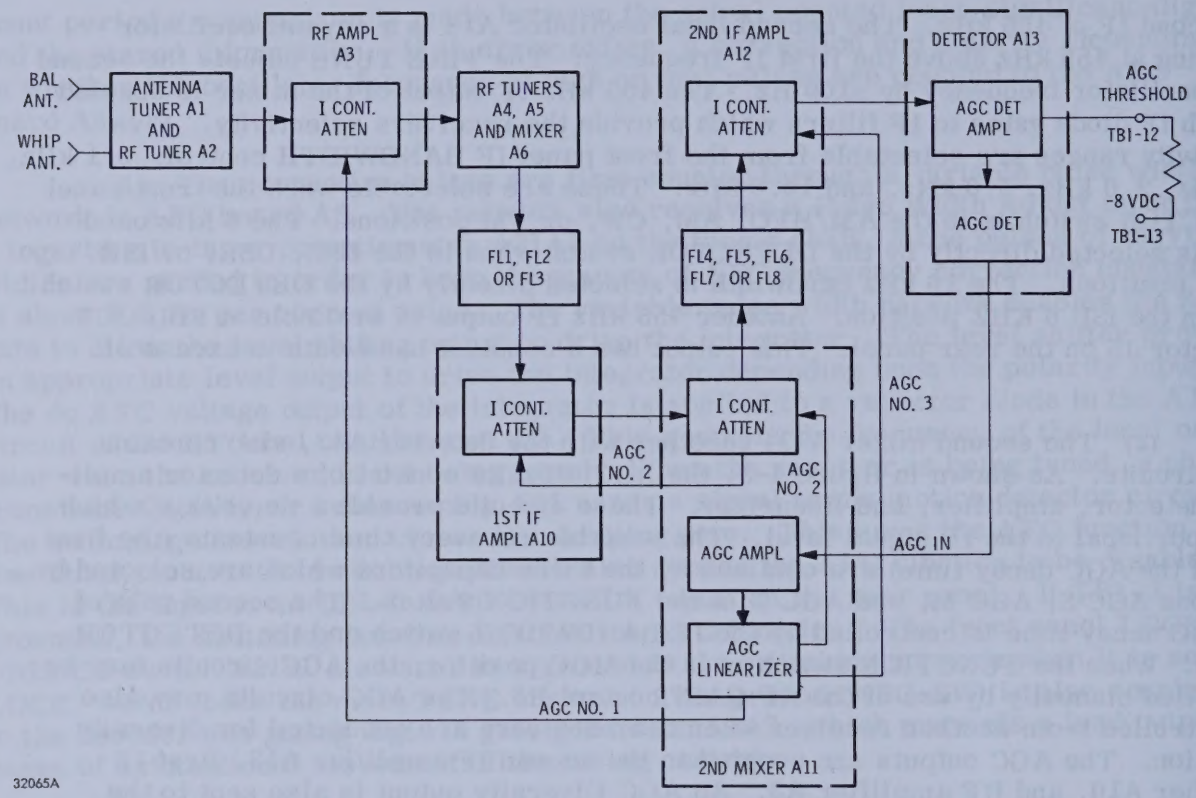


Figure 4-3. – AGC Loop, Simplified Block Diagram.

Table 4-2. - FUNCTION Switch S1.

SWITCH	POSITION	S1A (FRONT)	S1A (REAR)
1	OFF (shown)	No connection	No connection
2	STBY	Disables squelch circuit	Disconnects antenna inputs and turns off RF amplifier A3
3	AGC S	Disables squelch circuit	Enables slow decay time of receiver AGC
4	AGC M	Disables squelch circuit	Enables medium decay time of receiver AGC
5	AGC F	Disables squelch circuit	No connection. Allows for fast decay time of receiver AGC
6	MGC	Disables squelch circuit	Disables AGC circuit

Table 4-2. - FUNCTION Switch S1 - Continued.

SWITCH	POSITION	S1A (FRONT)	S1A (REAR)
7	SQUELCH	No connection. Enables squelch circuit silencing receiver noise during periods when no signal is received.	Enables medium decay time of receiver AGC

to AF amplifier A15. ISB reception is accomplished by use of both the USB and LSB product detectors; the USB detector drives the audio channel on the AF amplifier A15, and the LSB detector drives the audio channel on the ISB A14. The detector board also contains an AGC amplifier and detector. The AGC output is coupled to additional AGC circuits in the second mixer A11 (see figure 4-3). A carrier level output is also available from the carrier level detector, coupled to the CARRIER-LINE meter M1 via the CARRIER-OFF-LINE switch S5. This output supplements the carrier level output from the second mixer A11 for low level signal inputs to the receiver. The AGC threshold may be changed by experimentally inserting different valued resistors between AGC THRESHOLD terminals TB1-12 and TB1-13 on the rear panel.

(6) The AF amplifier board A15 provides audio amplification, noise limiting, and squelch control in all reception modes. The detected outputs from detector board A13 and ISB board A14 via DETECTOR switch S3A (front) and jumpered DET OUT and AUDIO IN terminals TB1-15 and TB1-14 are coupled to squelch and noise limiting circuits. The squelch circuit determines the signal-to-noise ratio and turns-on the attenuators on both the AF amplifier board A15 and ISB board A14, when the signal-to-noise ratio becomes low. The squelch sensitivity adjust control R14 sets the signal-to-noise ratio at which the squelch circuit will operate. FUNCTION switch S1A (front) disables the squelch circuit when in all positions except SQUELCH, and enables the squelch circuit when set to SQUELCH. The noise limiters, which are controlled by the NOISE LIMITER control, provide varying degrees of limiting to suppress noise.

(7) After the squelch and noise limiting circuits, audio amplifiers in both A15 and A14 provide line audio outputs at the rear panel. LINE GAIN controls adjust the gain of the line audio channels. Line audio is also coupled to the CARRIER-LINE LEVEL DB meter M1 via ISB MONITOR switch S2, DETECTOR switch S3A (rear), line meter amplifier and detector in IF amplifier A12, and CARRIER-OFF-LINE switch S5.

(8) The audio channel to be monitored at the front panel PHONES jack J7 and the PHONE AUDIO OUT terminal TB1-8 on the rear panel are selected by the ISB MONITOR switch S2 and DETECTOR switch S3C (rear). The ISB channel B audio output can only be selected when the DETECTOR switch is one of the ISB positions. In all other positions, only the main channel A audio output is available to the phone circuit. The audio output selected by the ISB monitor switch is coupled to the NAR-WIDE audio switch A17S1. Here an audio low-pass filter is either selected or bypassed before the signal enters the final audio and phones amplifiers. The AUDIO GAIN control determines the gain of the phone amplifier which couples the audio output to the front and rear panels.

Table 4-3. – DETECTOR Switch S3.

SWITCH POSITION	S3A (FRONT)	S3A (REAR)	S3B (FRONT)	S3B (REAR)	S3C (FRONT)	S3C (REAR)	DETECTION CAPABILITIES
1 AM/BFO (SHOWN)	AM detector output to main audio channel (CH A)	Main channel (CH A) LINE AUDIO output to CARRIER-LINE sw via line meter ampl. and detector	Turns-on XTAL BFO	Enables IF BANDWIDTH SW (BW control) and DSB gate	Enables IF BANDWIDTH SW (AGC delay cont.)	Connects main line audio (CH A) to ISB MONITOR sw	Same as for position 2 (AM) of DETECTOR switch, except uses crystal BFO. Used mainly for tuning monitor or frequency measurement.
2 AM	AM detector output to main audio channel (CH A)	Main channel (CH A) LINE AUDIO output to CARRIER-LINE sw via line meter ampl. and detector	No connection	Enables IF BANDWIDTH SW (BW control) and DSB gate	Enables IF BANDWIDTH SW (AGC delay cont.)	Connects main line audio (CH A) to ISB MONITOR sw	Amplitude modulated voice communication, double sideband, full carrier. Emission symbol A3. Telegraphy by the on-off keying of AM-AF, or AF, or by on-off keying of modulated emission. Emission symbol A2.
3 CW	CW detector output to main audio channel (CH A)	Main channel (CH A) LINE AUDIO output to CARRIER-LINE sw via line meter ampl. and detector	Turns-on Variable BFO	Enables IF BANDWIDTH SW (BW control) and DSB gate	Enables IF BANDWIDTH SW (AGC delay cont.)	Connects main line audio (CH A) to ISB MONITOR sw	Telegraphy by on-off keying without the use of a modulation audio frequency. Emission symbol A1. Telegraphy by frequency-shift keying without use of a modulating audio frequency; one of two frequencies being emitted at any instant. Emission symbol F1
4 LSB	LSB detector output to main audio channel (CH A)	Main channel (CH A) to CARRIER-LINE sw via line meter ampl. and detector	Turns-on XTAL BFO and enables LSB gate	Enables 6 kHz IF bandwidth	Enables AGC medium delay	Connects main line audio (CH A) to ISB MONITOR sw	Amplitude modulated voice communication, lower single sideband, reduced carrier. Emission symbol A3a.
5 USB	USB detector output to main audio channel (CH A)	Main channel (CH A) to CARRIER-LINE sw via line meter ampl. and detector	Turns-on XTAL BFO and enables USB gate	Enables 6 kHz IF bandwidth	Enables AGC medium delay	Connects main line audio (CH A) to ISB MONITOR sw	Amplitude modulated voice communication, upper sideband, reduced carrier. Emission symbol A3a.
6 ISB 3 KHZ	USB detector output to main audio channel (CH A)	Either CH A or CH B line audio output to (as above) depending upon ISB MONITOR SW position	Turns-on XTAL BFO	Enables 6 kHz IF bandwidth and DSB gate	Enables AGC fast delay	Connects ISB line audio (CH B) to ISB MONITOR sw	Amplitude modulated voice communication, two independent sidebands, reduced carrier. Emission symbol A3b.
7 ISB 6 KHZ	USB detector output to main audio channel (CH A)	Either CH A or CH B line audio output to (as above) depending upon ISB MONITOR	Turns-on XTAL BFO and enables 16 kHz IF bandwidth sw position.	Enables DSB gate	Enables AGC fast delay	Connects ISB line audio (CH B) to ISB MONITOR sw	Amplitude modulated voice communication, two independent sidebands. Emission symbol A9b.
8 FM	FM detector output to main audio channel (CH A)	Same as for position 1	Enables IF BANDWIDTH sw (BW control	Enables DSB gate	Same as for position 1	Same as for position 1	Frequency modulated voice communication. Emission symbol F3.

4-3. POWER DISTRIBUTION. - See figure 4-4 for a power distribution diagram. Four dc voltages (+5V, -8V, +25V and +230V) are distributed to circuits in the receiver with the appropriate ac or dc input at J1 (refer to paragraph 4-4q and r) when the FUNCTION switch is in any position except the OFF position. A precision dc voltage is provided from the second local oscillator A18 for the FINE TUNE control. The first local oscillator A7 and the counter A9 receive +25V through the diversity switch A16S1 on the connector assembly A16 when switch A16S1 is set to NORMAL. When switch A16S1 is set to DIVERSITY, the first local oscillator A7 and the counter A9 may be momentarily turned-on by setting the DIV TUNE-ANT DSBL switch S4 to DIV TUNE. The FUNCTION switch S1A will supply +25V to AF amplifier A15 when in all positions except OFF and SQUELCH.

4-4. FUNCTIONAL OPERATION OF ELECTRONIC CIRCUITS.

a. Electrical RF Connector Assembly A16. - (See figure A-4 for a schematic diagram.) This assembly consists basically of an interconnection board (mother board), six connectors, and a diversity switch. Printed circuit boards A1, A2, and A4 through A7 are installed in the connectors on the interconnection board. Most of the interconnections within the RF section are provided by the interconnection board. The NORMAL-DIVERSITY switch S1 is provided to allow for diversity reception. When switch S1 is in the NORMAL position (single receiver operation or the receiver is used as the master receiver, when two receivers are connected for diversity reception), +25 vdc turn-on voltage is available at the first local oscillator (LO) A7 and at counter A9. The LO output signal is coupled to the first mixer A6 and LOC OSC IN/OUT connector J4 on the rear panel. When S1 is in the DIVERSITY position, +25 vdc is removed from first LO A7 and counter A9, and the LOC OSC IN/OUT connector J4 is connected to the LO input of first mixer to allow for use of an external LO signal. Plus 25 vdc may be momentarily connected to first LO A7 and counter A9 by use of the DIV TUNE position of switch S4 for tuning purposes.

b. Antenna Tuner A1. - (See figure A-5 for a schematic diagram.) The antenna tuner contains one-half of five different RF double-tuned filters, two wafers of the band switch, a relay for terminating the whip and low impedance antenna inputs, and a neon lamp for suppressing large input signals.

(1) A low impedance (72-ohm) antenna input is coupled in at pins 9, K and through contacts B3 and B2 of antenna relay K1 to terminal 18 of switch S1A. Antenna relay K1 is activated by grounding the antenna relay K1 ground return line, which is controlled by front panel ANT-DSBL switch S4 or FUNCTION switch S1 when in STBY position. This opens both antenna input circuits, connects the antenna tuner input to ground and removes +25 vdc from the RF amplifier (pins 8, J). The resulting attenuation is over 60 db.

(2) Switch S1 is shown in the band 1 position, so that contact 13 is connected to the low impedance input. Transformer T1 is a 4:1 impedance converter for proper matching with the first double-tuned filter for band 1, half of which is comprised of L17, L18, L19, L20, C7, C2, and one section of the air-variable tuning capacitor. L19 and C7 are used to align the band 1 filter at the band edges. An identical half of the filter is located on the RF tuner board A2. See figure 4-2 for a simplified schematic of the double-tuned filter. The air-variable tuning capacitor is connected through contact 19 of switch S1A for tuning band 1 from 1.48 MHz to 2.80 MHz. The output for band 1 at pin 3, C is returned to the mother board for proper interconnection to board A2.

(3) The whip antenna input is coupled in at pin 11, M and passes through contacts A3 and A2 of antenna disabling relay A1K1 and then through part of BAND-MHZ switch S1A to the whip antenna tuning circuit which is part of the antenna trimming circuit. A different coil (L21 through L25) is used for each band and the circuit is tuned by the antenna trimmer capacitor to provide maximum coupling into the first double-tuned filter. The antenna trimmer capacitor is mounted at the front panel and is electrically connected to board A1 at connector J1. Capacitor C1 couples the signal to the first double-tuned filter at the tuning capacitor input point.

(4) The remaining four bands function exactly the same as band 1, but without a transformer for impedance transformation. Section B of switch S1 grounds all unused contacts of section A to prevent unwanted resonance.

(5) A neon lamp DS1 is connected across the RF filter tank circuits to suppress large input signals from damaging the input circuitry of the receiver. An antenna input level of approximately 8 volts peak will cause the lamp to turn on. This, in turn, loads the tank circuit and prevents higher voltage levels to appear across the input tank circuit.

c. RF Tuners A2, A4, and A5. - (See figure A-6 for a schematic diagram.) There are three RF tuner boards used in the receiver, all of which are identical. Each board contains one-half of five different RF double-tuned filters which are band switched using switch S1. As indicated in the discussion of antenna tuner board (A1), (refer to paragraph 4-4b.) L18, L19, L20, L21, C7, C2, C1, and one section of the air-variable tuning capacitor comprise the band 1 filter.

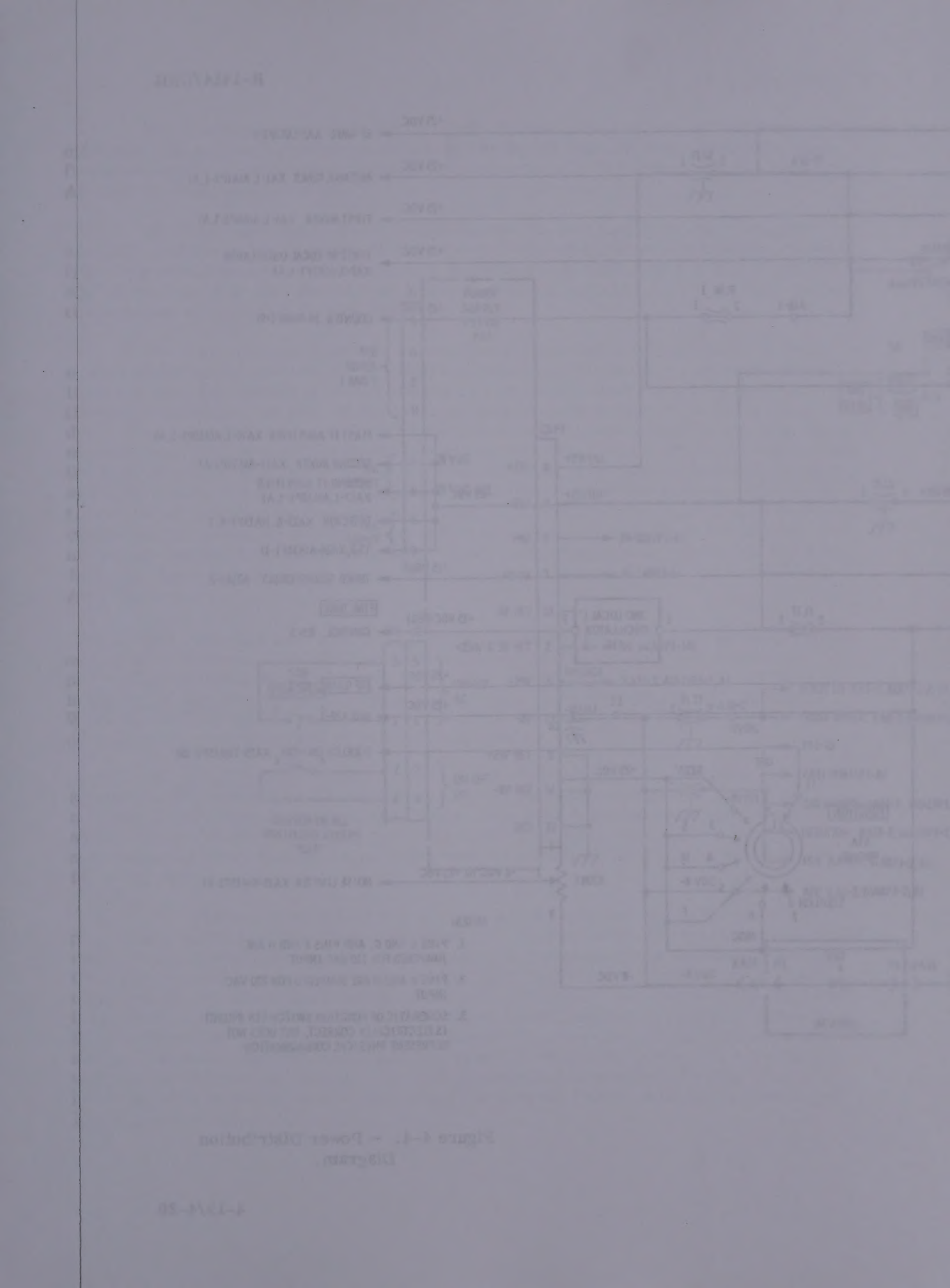
(1) The schematic shows that a signal for band 1 enters at pins 3, C and goes through the filter circuit to impedance-matching transformer T1, to contact 13 on S1A, then out wiper contact 18 to the in/out pins 11, M.

(2) The air-variable tuning capacitor is connected in through pins 15, S to switch S1A wiper contact 6. For band 1, contact 1 of switch S1A connects the tuning capacitor to the band 1 filter circuitry. As the switch is rotated, the in/out pins 11, M are switched to any one of the five RF bands as is the tuning capacitor. The first RF double-tuned filter is formed by the A2 board in conjunction with the A1 board. (See figure 4-2.) The output impedance of the RF tuner board A2 is at 72 ohms which matches the input impedance of the RF amplifier board A3.

(3) RF tuner boards A4 and A5 comprise the second RF double-tuned filter which further filters the RF signal. The mother board interconnects these two boards as shown in figure 4-2.

(4) For band 1, the RF signal enters the board A4 at pins 11, M and connects to transformer T1 through switch S1A. The signal then passes through the filter circuit (L18, L19, L20, L21, C7, and the tuning capacitor) to pin 3, C. Pin 3, C on board A4 is connected to pin 3, C on the board A5. The signal passes through the filter circuit (L18, L19, L20, L21, and C7) on board A5 and the tuning capacitor to transformer T1.

d. Tuner Subassembly A21. - (See figure A-7 for a schematic diagram.) The tuner subassembly A21 consists of the tuning capacitor, a logarithmic-taper potentiometer, a motion detector circuit, and a dial lock switch.



(3) The whip antenna input is coupled in at pin 11, M and passes through contacts A3 and A2 of antenna disabling relay A1K1 and then through part of BAND-MHZ switch S1A to the whip antenna tuning circuit which is part of the antenna trimming circuit. A different coil (L21 through L25) is used for each band and the circuit is tuned by the antenna trimmer capacitor to provide maximum coupling into the first double-tuned filter. The antenna trimmer capacitor is mounted at the front panel and is electrically connected to board A1 at connector J1. Capacitor C1 couples the signal to the first double-tuned filter at the tuning capacitor input point.

(4) The remaining four bands function exactly the same as band 1, but without a transformer for impedance transformation. Section B of switch S1 grounds all unused contacts of section A to prevent unwanted resonance.

(5) A neon lamp DS1 is connected across the RF filter tank circuits to suppress large input signals from damaging the input circuitry of the receiver. An antenna input level of approximately 8 volts peak will cause the lamp to turn on. This, in turn, loads the tank circuit and prevents higher voltage levels to appear across the input tank circuit.

c. RF Tuners A2, A4, and A5. - (See figure A-6 for a schematic diagram.) There are three RF tuner boards used in the receiver, all of which are identical. Each board contains one-half of five different RF double-tuned filters which are band switched using switch S1. As indicated in the discussion of antenna tuner board (A1), (refer to paragraph 4-4b.) L18, L19, L20, L21, C7, C2, C1, and one section of the air-variable tuning capacitor comprise the band 1 filter.

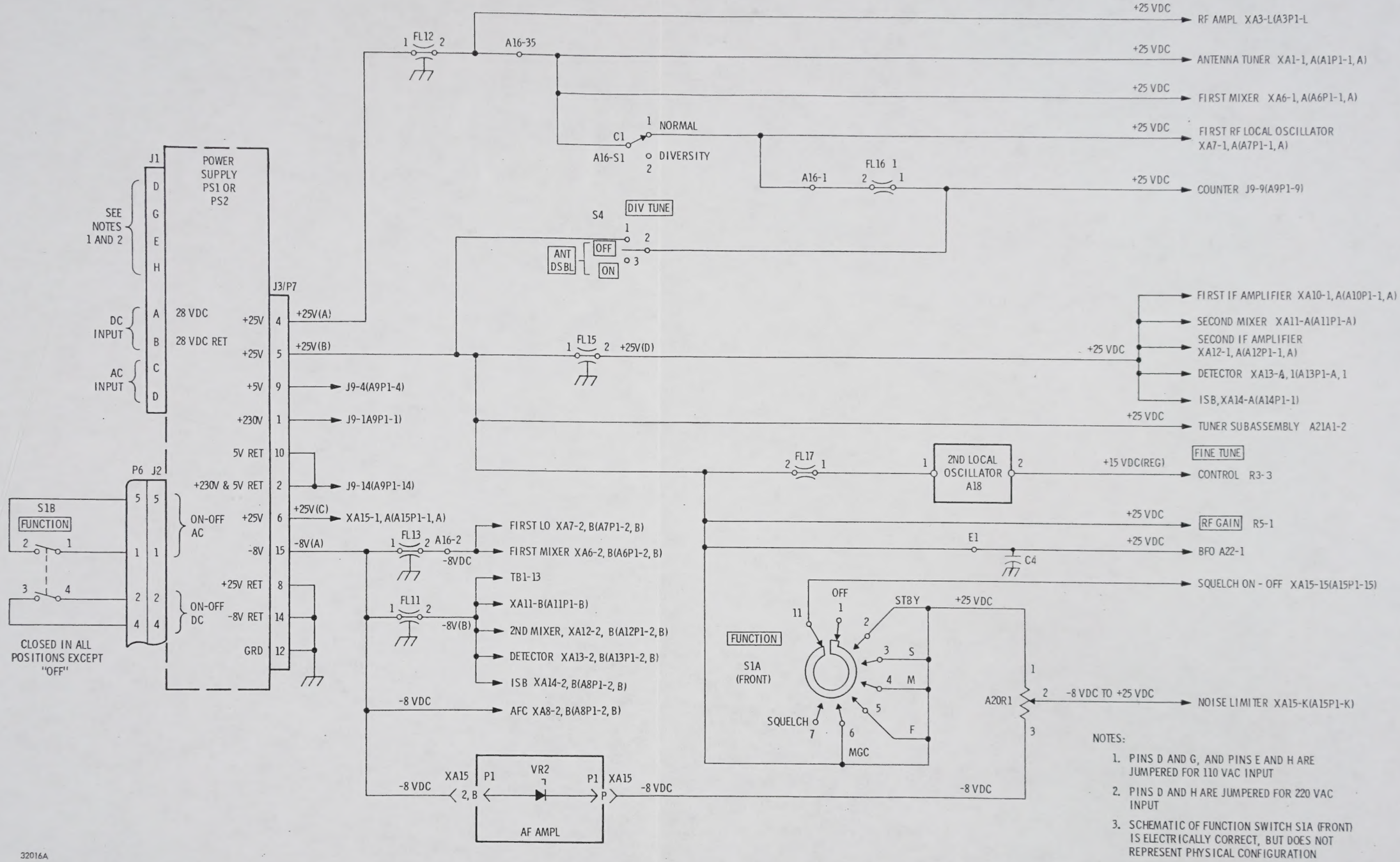
(1) The schematic shows that a signal for band 1 enters at pins 3, C and goes through the filter circuit to impedance-matching transformer T1, to contact 13 on S1A, then out wiper contact 18 to the in/out pins 11, M.

(2) The air-variable tuning capacitor is connected in through pins 15, S to switch S1A wiper contact 6. For band 1, contact 1 of switch S1A connects the tuning capacitor to the band 1 filter circuitry. As the switch is rotated, the in/out pins 11, M are switched to any one of the five RF bands as is the tuning capacitor. The first RF double-tuned filter is formed by the A2 board in conjunction with the A1 board. (See figure 4-2.) The output impedance of the RF tuner board A2 is at 72 ohms which matches the input impedance of the RF amplifier board A3.

(3) RF tuner boards A4 and A5 comprise the second RF double-tuned filter which further filters the RF signal. The mother board interconnects these two boards as shown in figure 4-2.

(4) For band 1, the RF signal enters the board A4 at pins 11, M and connects to transformer T1 through switch S1A. The signal then passes through the filter circuit (L18, L19, L20, L21, C7, and the tuning capacitor) to pin 3, C. Pin 3, C on board A4 is connected to pin 3, C on the board A5. The signal passes through the filter circuit (L18, L19, L20, L21, and C7) on board A5 and the tuning capacitor to transformer T1.

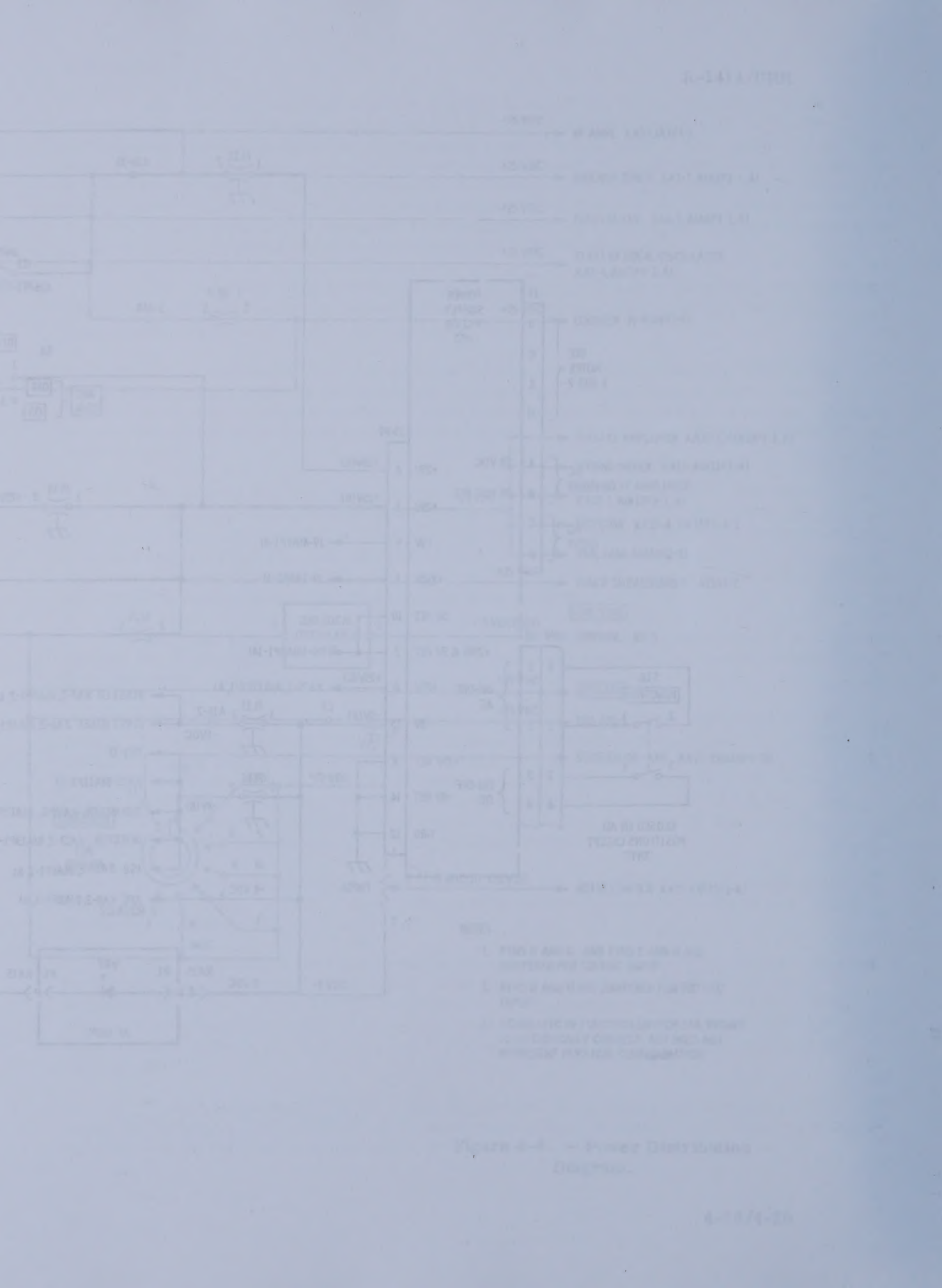
d. Tuner Subassembly A21. - (See figure A-7 for a schematic diagram.) The tuner subassembly A21 consists of the tuning capacitor, a logarithmic-taper potentiometer, a motion detector circuit, and a dial lock switch.



NOTES:

1. PINS D AND G, AND PINS E AND H ARE JUMPERED FOR 110 VAC INPUT
2. PINS D AND H ARE JUMPERED FOR 220 VAC INPUT
3. SCHEMATIC OF FUNCTION SWITCH S1A (FRONT) IS ELECTRICALLY CORRECT, BUT DOES NOT REPRESENT PHYSICAL CONFIGURATION

Figure 4-4. – Power Distribution Diagram.



(1) The tuning capacitor C1 is a gear-driven, five section, air-variable capacitor that accomplishes the main tuning for the RF section of the receiver. The five sections are electrically coupled to antenna tuner A1, RF tuners A2, A4, and A5, and RF local oscillator A7.

(2) The logarithmic-taper potentiometer R1 is mounted on the tuner subassembly and the wiper is driven by the tuning shaft. The Pulse Width Adjust output from this potentiometer is connected to a variable pulse width network in AFC board A8. This is used to vary the correct pulse in order to keep the AFC frequency correction constant at about 3.5 Hz per correct pulse.

(3) The motion detector is a sensitive electro-optical device used to sense motion of the tuning knob shaft. A pattern of alternate transparent and opaque radial lines are near the outside of a disc attached to the tuning shaft. Light is passed through a fixed array of slits of the same pattern is close proximity to the moving disc. Photo transistor Q1 provides an electrical output proportional to the light transmission from DS1 through the fixed slits and moving disk. Light transmission through the fixed and moving patterns will vary from near zero to maximum and back to zero again for motion of an amount equal to the repetition cycle of the pattern. The phototransistor Q1 drives a motion detector circuit in AFC board A8. The motion detector circuit in AFC board A8 determines whether or not the tuning knob is rotating by noting any change in the phototransistor signal, indicating motion, and stops the AFC function. Once motion stops, the motion detector circuit notes this and enables the AFC function.

(4) The dial lock switch S1 provides an additional means of manually turning on the AFC function. The LOCK-UNLOCK control on the receiver front panel is physically connected to the dial lock switch S1. When the LOCK-UNLOCK control is in the LOCK position dial lock switch S1 is closed. This freezes the AFC memory. When the LOCK-UNLOCK control is in the UNLOCK position the dial lock switch S1 is open allowing manual control of receiver frequency.

e. RF Amplifier A3. - (See figure 4-5 for a block diagram and figure A-8 for a schematic diagram.) The RF amplifier A3 provides a nominal gain of 14 db, and a nominal 72-ohm input and output impedance for proper termination of the first and second double-tuned filters. An externally controlled attenuator circuit provides approximately 30 db of attenuation to prevent saturation of the RF amplifier and the following circuit.

(1) The output of the RF tuner board A2 is connected to the RF amplifier, pin S, via a coaxial cable. Test point J2 at this input provides for measurement of the relative signal level through R1. The signal is AC coupled to the attenuator through C8. The attenuator consists of diodes CR1, CR2, and CR3 as variable shunt resistors, and R2 and R3 as fixed series resistors. Capacitor C11 compensates for stray inductance so that attenuation versus frequency curve remains essentially constant. Direct current is applied to pin N and is filtered by a low-pass filter consisting of C6 and L4. As more current is applied, the variable resistance diodes start to conduct, which reduces their resistance. The current supplied is controlled by the IF signal level; circuits in the IF section also shape the current characteristics to provide for linear gain control.

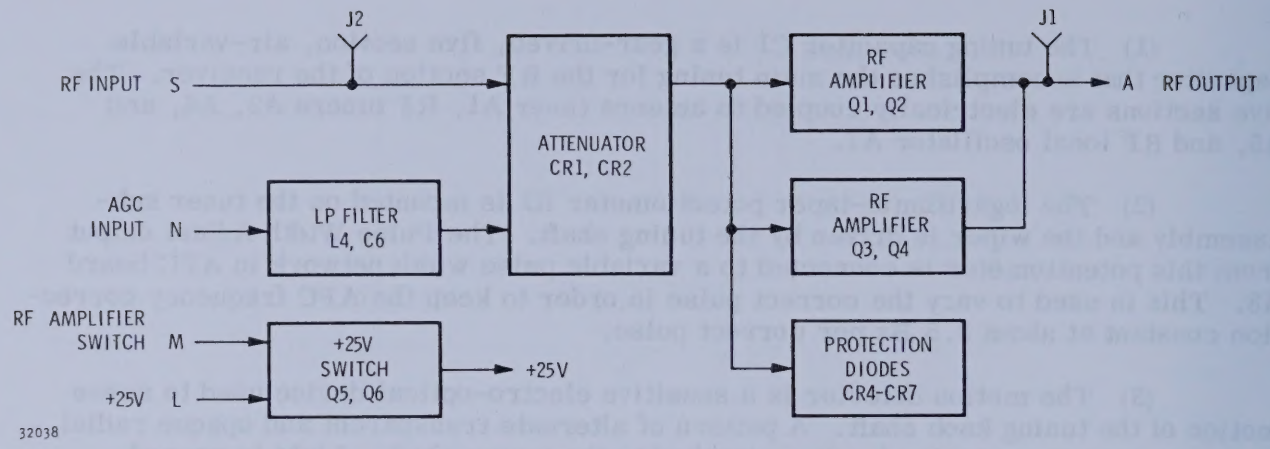


Figure 4-5. – RF Amplifier A3, Block Diagram.

(2) Capacitor C12 ac-couples the signal to diodes CR4, CR5, CR6, and CR7. These diodes are used to protect the amplifier when signal levels reach approximately 1.2 volts peak-to-peak.

(3) The amplifier section consists of two identical, parallel connected, two-stage amplifiers. One-half of the input signal current is ac-coupled through C13 to the base of Q1, a low-noise, wideband transistor amplifier. Q1 is connected in a common-emitter configuration. The amplified signal at the collector of Q1 is directly coupled to the base of Q2, which is connected in a common-collector configuration. The amplifier characteristics are stabilized by voltage feedback using R8 and current feedback using R5 and R6. The feedback also determines the gain and input/output impedances. Coil C7 is a high-frequency suppressor that guarantees the absolute stability of the amplifier.

(4) Transistors Q3 and Q4 and associated components form an amplifier identical to that described above. The parallel connection of the two amplifiers provides twice as much dynamic range as one amplifier. The outputs of Q2 and Q4 are coupled together with a resistive attenuator consisting of R11, R12, R20, R21 and R22. The output of the RF amplifier at pin A can be monitored at test point J1 through R13 and is connected via a coaxial cable to the RF tuner board A4.

(5) Transistors Q5 and Q6 are used as a switch to deactivate all circuits on the RF amplifier board A3 by removing +25 vdc when the DIV TUNE-ANT DSBL switch S4 is set to ON or when the FUNCTION switch S1 is set to STBY.

f. First Mixer A6. - (See figure 4-6 for a block diagram and figure A-9 for a schematic diagram.) The first mixer board A6 contains a LO amplifier, a doubly-balanced push-pull, class B linear converter, a band wafer switch, and three tunable output transformers.

(1) The LO input at pin D is coupled through resistive pad (R10, R11, R12) to a wide-band amplifier consisting of Q5 and Q6. Transistor Q5 is connected in a common-emitter configuration and the collector of Q5 is directly coupled to the base of Q6, which is connected in the common-collector configuration. The amplifier characteristics are stabilized by use of voltage feedback using R18 and current feedback

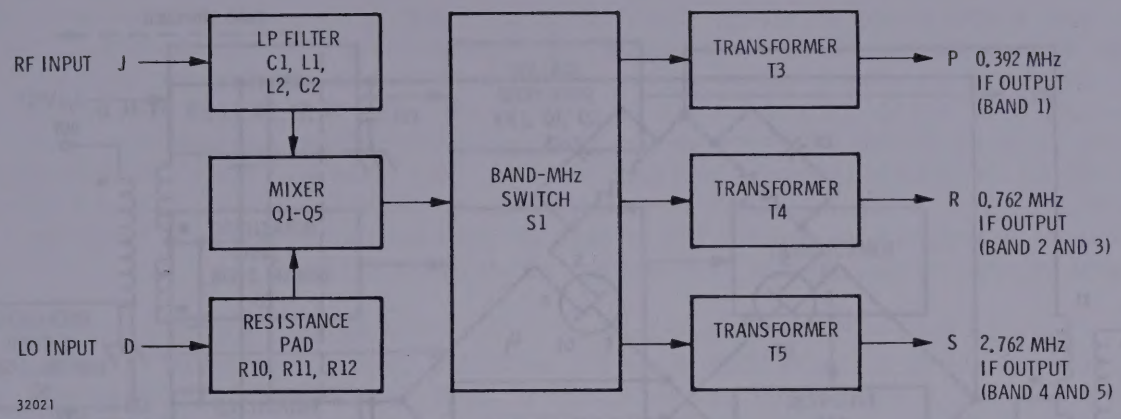

RF INPUT J
LP FILTER C1, L1, L2, C2
MIXER Q1-Q5
RESISTANCE PAD R10, R11, R12
LO INPUT D
BAND-MHz SWITCH S1
TRANSFORMER T3
TRANSFORMER T4
TRANSFORMER T5
P 0.392 MHz IF OUTPUT (BAND 1)
R 0.762 MHz IF OUTPUT (BAND 2 AND 3)
S 2.762 MHz IF OUTPUT (BAND 4 AND 5)
32021

Figure 4-6. – First Mixer A6, Block Diagram.

using R13 and R14. The feedback also determines the gain and input/output impedances. The output of the LO amplifier is coupled to the primary of T2 through C21. The secondary of T2 has two outputs which are 180 degrees out of phase, and each output is used to drive two of the four transistors that make up the mixer circuit (see figure 4-7). At any one time, two transistors are biased off and two are biased in their active linear region. The RF input at pin J is coupled through a low-pass filter (C1, C2, L1, L2) to the primary of T1. The filter is used to prevent harmonics of the first LO at frequencies greater than 100 MHz from being fed back to the antenna. The secondary of T1 has two outputs which are 180 degrees out of phase. Each output of T1 is coupled to the inputs of two of the four mixer circuit transistors; pin 5 to Q1 and Q2, and pin 3 to Q3 and Q4.

(2) The transistors are matched and selected for their square-law characteristics of bias voltage (Vgs) versus current (Ids). The action of the LO voltage on the bias voltage creates a square-law mixing action on the RF signal. Due to balancing effects on the input and output, the LO signal level is suppressed at these ports. In addition, all even-order spurious responses are balanced at the output port.

(3) The outputs of Q1 and Q4 are connected in parallel and connect to wiper No. 24 of BAND-MHZ switch S1. Similarly, the outputs of Q2 and Q3 are connected in parallel and connect to wiper No. 19 of BAND-MHZ switch S1. The switch is shown in the band 1 position which connects the primary winding of T3 to the parallel outputs of the mixer transistors. Capacitors C10, C19, C11, and C13 resonate with T3 at the IF frequency of 0.392 MHz. The IF is coupled to the secondary of T3, which has a nominal impedance of 500 ohms. This impedance provides the proper loading for the first IF filters.

(4) Switch S1 is used to select the proper output tuned circuit and is dependent on the band selected by the front panel BAND-MHZ switch. Bands 2 and 3 use transformer T4, and bands 4 and 5 use transformer T5. Inductors L4 and L5 are used to suppress resonant frequencies which occur due to the leakage inductance of T4 and T5 at particular LO frequencies. These resonances would produce excessive LO signal at the IF output ports.

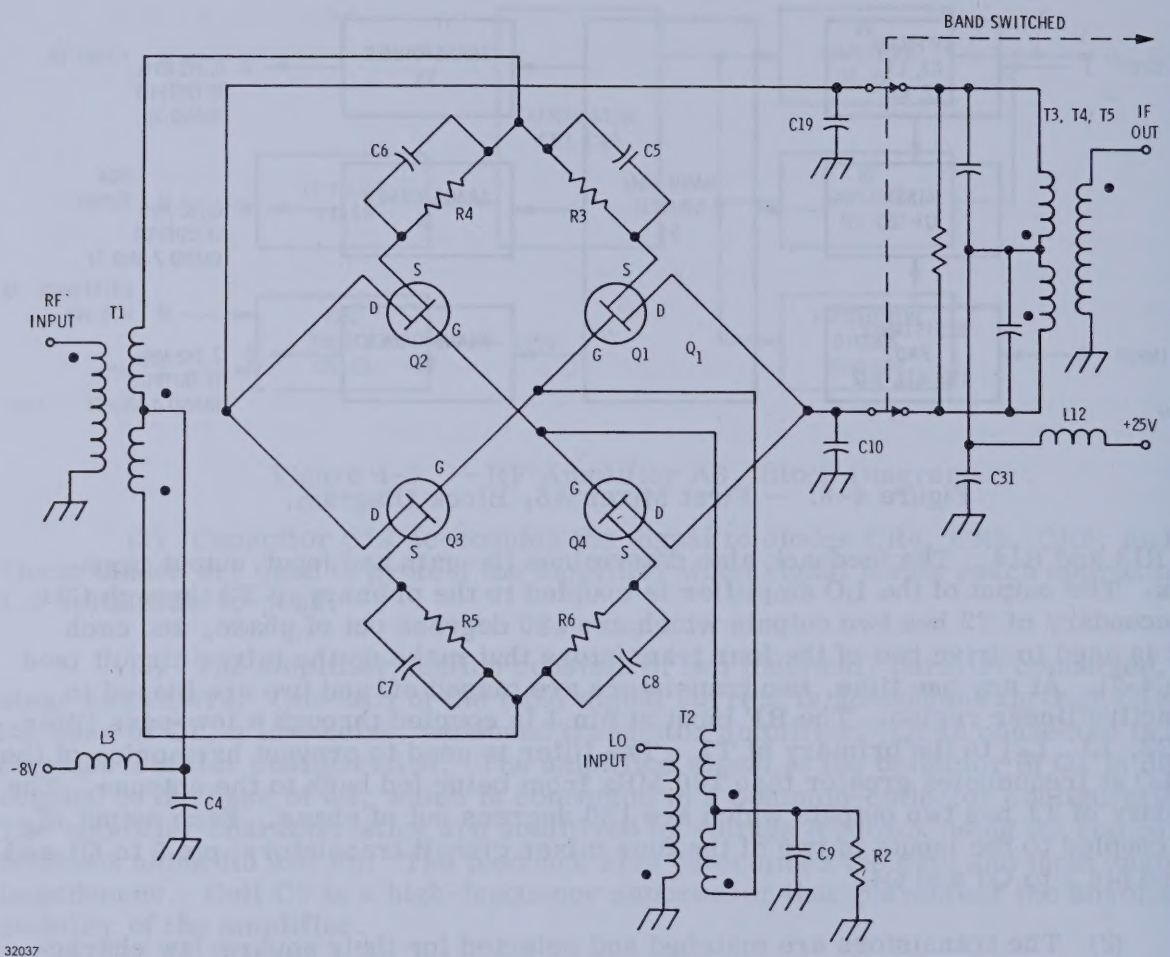


Figure 4-7. – First Mixer A6, Simplified Schematic Diagram.

(5) Power for the mixer is supplied by two voltages, +25V and -8V. The +25 volt line has RF decoupling consisting of C31, C32, C33, C34, L12, L13, L14, and L15. The -8 volt line has decoupling for audio as well as for RF. This is necessary to prevent undesired audio modulation on the -8 volt line from entering and affecting receiver operation.

g. First Local Oscillator A7A1. - (See figure 4-8 for a block diagram and figure A-10 for a schematic diagram.) The local oscillator is a conventional Hartley configuration using a common-gate field effect transistor (FET) amplifier as the active element. Five completely separate oscillator circuits (Q5-Q8) are used and BAND-MHZ switch S1 selects the proper frequency range. Common-base buffer amplifiers Q3 and Q4 provide three isolated outputs: one to drive the mixer, one for the counter, and a third for the rear panel LOC OSC IN/OUT connector J4.

(1) Switch section S1A is shown in the band 1 position with contact 13 connecting the output of the band 1 oscillator at C18 to the switch wiper No. 18 which is connected to pin 5 of transformer T1. The remaining wiper No. 1 of S1A connects the stator of the tuning capacitor A21C1 to the oscillator tank circuit, pin 4 of L5, via

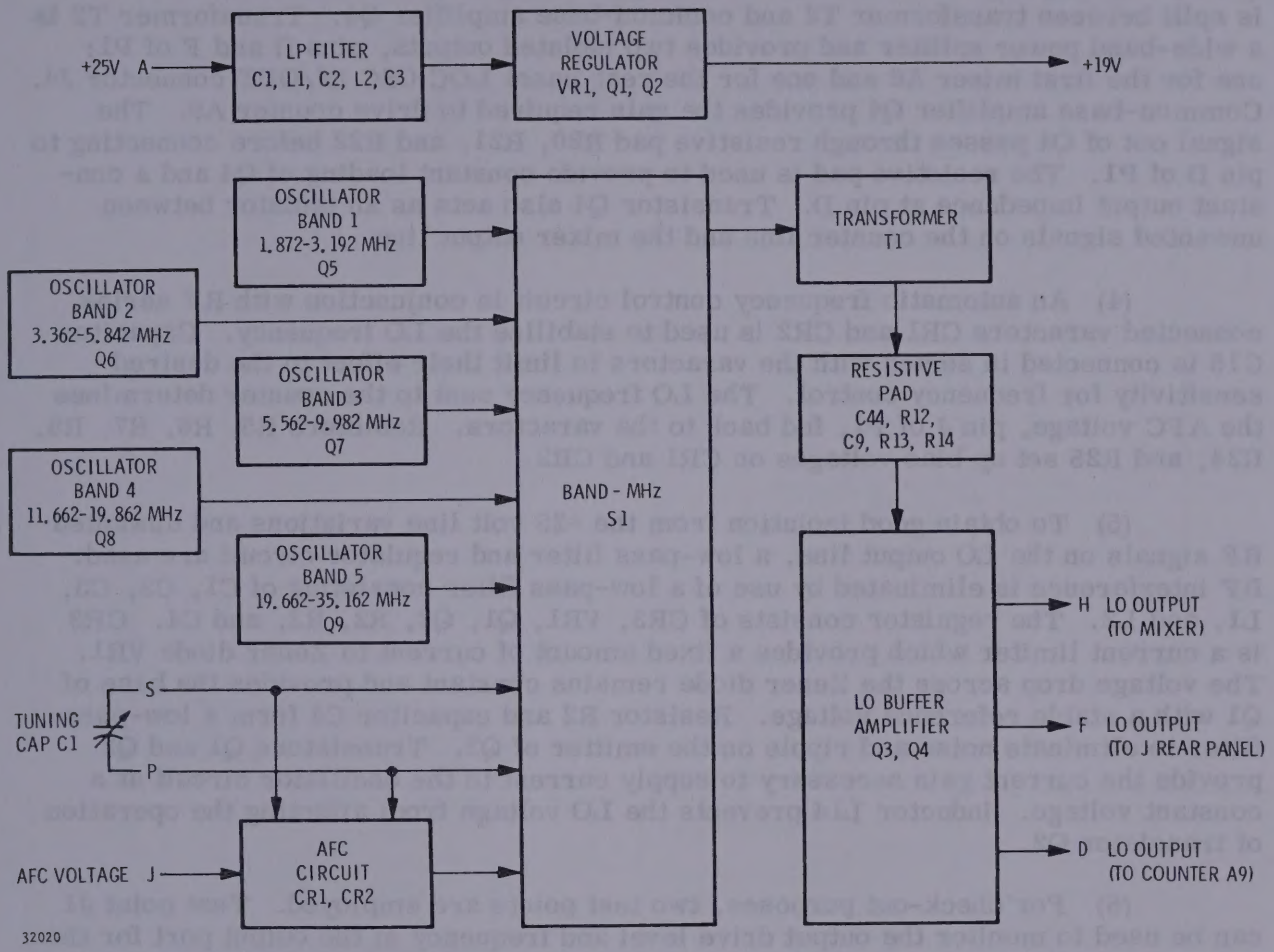


Figure 4-8. – First Local Oscillator A7A1.

connector P1, pin S. The rotor of the tuning capacitor connects to pin 1 of L5 via connector P1, pin P. The unused oscillator tank circuits are RF shorted by C43 and switch section S1B; S1B also shorts the outputs of all unused oscillators to this same reference. This assures that no stray resonances or oscillations occur in the desired band of operation.

(2) Inductor L5 and capacitor C19, C20, and C21, along with the tuning capacitor, make up the frequency-determining elements of the band 1 oscillator. Capacitor C19 is used as a temperature compensating element; L5 and C21 are adjustable and allow the frequency of oscillation to be adjusted to the band edges. C20 is a padder for three-point tracking between the RF filters and the LO. L4 is used to suppress undesired oscillations due to stray capacitance and the leakage inductance of L5. The remaining bands are identical in configuration and, as switch S1 is rotated, will perform exactly as described for band 1.

(3) As mentioned in paragraph 4-4g(1), the outputs of the oscillator are connected to the primary of transformer T1. The signal coupled to the secondary of T1 passes through a resistive pad, R12, R13, R14 to the emitter of common-base

amplifier Q3. The resistive pad provides a constant load on the oscillator for frequency and output power stability. The amplified signal power at the collector of Q3 is split between transformer T2 and common-base amplifier Q4. Transformer T2 is a wide-band power splitter and provides two isolated outputs, pins H and F of P1: one for the first mixer A6 and one for the rear panel LOC OSC IN/OUT connector J4. Common-base amplifier Q4 provides the gain required to drive counter A9. The signal out of Q4 passes through resistive pad R20, R21, and R22 before connecting to pin D of P1. The resistive pad is used to provide constant loading of Q4 and a constant output impedance at pin D. Transistor Q4 also acts as an isolator between unwanted signals on the counter line and the mixer output line.

(4) An automatic frequency control circuit in conjunction with RF series connected varactors CR1 and CR2 is used to stabilize the LO frequency. Capacitor C15 is connected in series with the varactors to limit their effect to the desired sensitivity for frequency control. The LO frequency sent to the counter determines the AFC voltage, pin J of P1, fed back to the varactors. Resistors R5, R6, R7, R8, R24, and R25 set up bias voltages on CR1 and CR2.

(5) To obtain good isolation from the +25 volt line variations and unwanted RF signals on the LO output line, a low-pass filter and regulator circuit are used. RF interference is eliminated by use of a low-pass filter consisting of C1, C2, C3, L1, and L2. The regulator consists of CR3, VR1, Q1, Q2, R2, R3, and C4. CR3 is a current limiter which provides a fixed amount of current to Zener diode VR1. The voltage drop across the Zener diode remains constant and provides the base of Q1 with a stable reference voltage. Resistor R2 and capacitor C4 form a low-pass filter to eliminate noise and ripple on the emitter of Q2. Transistors Q1 and Q2 provide the current gain necessary to supply current to the oscillator circuit at a constant voltage. Inductor L14 prevents the LO voltage from affecting the operation of transistor Q2.

(6) For check-out purposes, two test points are employed. Test point J1 can be used to monitor the output drive level and frequency at the output port for the counter, pin D of P1. Thes point J2 can be used to monitor the DC voltage level at the collector of Q2 for proper regulator operation.

h. AFC and Electronic Digital Readout Counter, A8 and A9. - See figure 4-9 for a block diagram and figure 4-10 for a timing diagram of the frequency counter and AFC circuits. See figure A-11 for an interconnection diagram of the counter. The counter uses integrated circuits for logic elements. Refer to paragraph 4-4h(4) for a listing of these integrated circuits and explanations of their use. To provide direct readout of the tuned frequency, the counter is preset to subtract the intermediate frequency from the count. Six digits are displayed; the most-significant-digit represents tens of megahertz and the least-significant-digit represents hundreds of hertz. The readout accuracy is determined by the precision of the reference oscillator standard. The oscillator is a 1 MHz crystal reference oscillator with frequency stability better than ±1 Hz over the temperature range 0°C to 75°C. This standard reference oscillator is divided down to develop the basic 50 Hz count rate. A gate generator circuit develops several basic timing waveforms which control the reset, preset, count interval, and display intervals required to cause the counter to repetitively display the tuned frequency 50 times per second.

The AFC function provides for locking the frequency of the local oscillator to the reference oscillator of the counter. It is important to understand that the AFC function

amplifier Q3. The resistive pad provides a constant load on the oscillator for frequency and output power stability. The amplified signal power at the collector of Q3 is split between transformer T2 and common-base amplifier Q4. Transformer T2 is a wide-band power splitter and provides two isolated outputs, pins H and F of P1: one for the first mixer A6 and one for the rear panel LOC OSC IN/OUT connector J4. Common-base amplifier Q4 provides the gain required to drive counter A9. The signal out of Q4 passes through resistive pad R20, R21, and R22 before connecting to pin D of P1. The resistive pad is used to provide constant loading of Q4 and a constant output impedance at pin D. Transistor Q4 also acts as an isolator between unwanted signals on the counter line and the mixer output line.

(4) An automatic frequency control circuit in conjunction with RF series connected varactors CR1 and CR2 is used to stabilize the LO frequency. Capacitor C15 is connected in series with the varactors to limit their effect to the desired sensitivity for frequency control. The LO frequency sent to the counter determines the AFC voltage, pin J of P1, fed back to the varactors. Resistors R5, R6, R7, R8, R24, and R25 set up bias voltages on CR1 and CR2.

(5) To obtain good isolation from the +25 volt line variations and unwanted RF signals on the LO output line, a low-pass filter and regulator circuit are used. RF interference is eliminated by use of a low-pass filter consisting of C1, C2, C3, L1, and L2. The regulator consists of CR3, VR1, Q1, Q2, R2, R3, and C4. CR3 is a current limiter which provides a fixed amount of current to Zener diode VR1. The voltage drop across the Zener diode remains constant and provides the base of Q1 with a stable reference voltage. Resistor R2 and capacitor C4 form a low-pass filter to eliminate noise and ripple on the emitter of Q2. Transistors Q1 and Q2 provide the current gain necessary to supply current to the oscillator circuit at a constant voltage. Inductor L14 prevents the LO voltage from affecting the operation of transistor Q2.

(6) For check-out purposes, two test points are employed. Test point J1 can be used to monitor the output drive level and frequency at the output port for the counter, pin D of P1. Thes point J2 can be used to monitor the DC voltage level at the collector of Q2 for proper regulator operation.

h. AFC and Electronic Digital Readout Counter, A8 and A9. - See figure 4-9 for a block diagram and figure 4-10 for a timing diagram of the frequency counter and AFC circuits. See figure A-11 for an interconnection diagram of the counter. The counter uses integrated circuits for logic elements. Refer to paragraph 4-4h(4) for a listing of these integrated circuits and explanations of their use. To provide direct readout of the tuned frequency, the counter is preset to subtract the intermediate frequency from the count. Six digits are displayed; the most-significant-digit represents tens of megahertz and the least-significant-digit represents hundreds of hertz. The readout accuracy is determined by the precision of the reference oscillator standard. The oscillator is a 1 MHz crystal reference oscillator with frequency stability better than ±1 Hz over the temperature range 0°C to 75°C. This standard reference oscillator is divided down to develop the basic 50 Hz count rate. A gate generator circuit develops several basic timing waveforms which control the reset, preset, count interval, and display intervals required to cause the counter to repetitively display the tuned frequency 50 times per second.

The AFC function provides for locking the frequency of the local oscillator to the reference oscillator of the counter. It is important to understand that the AFC function

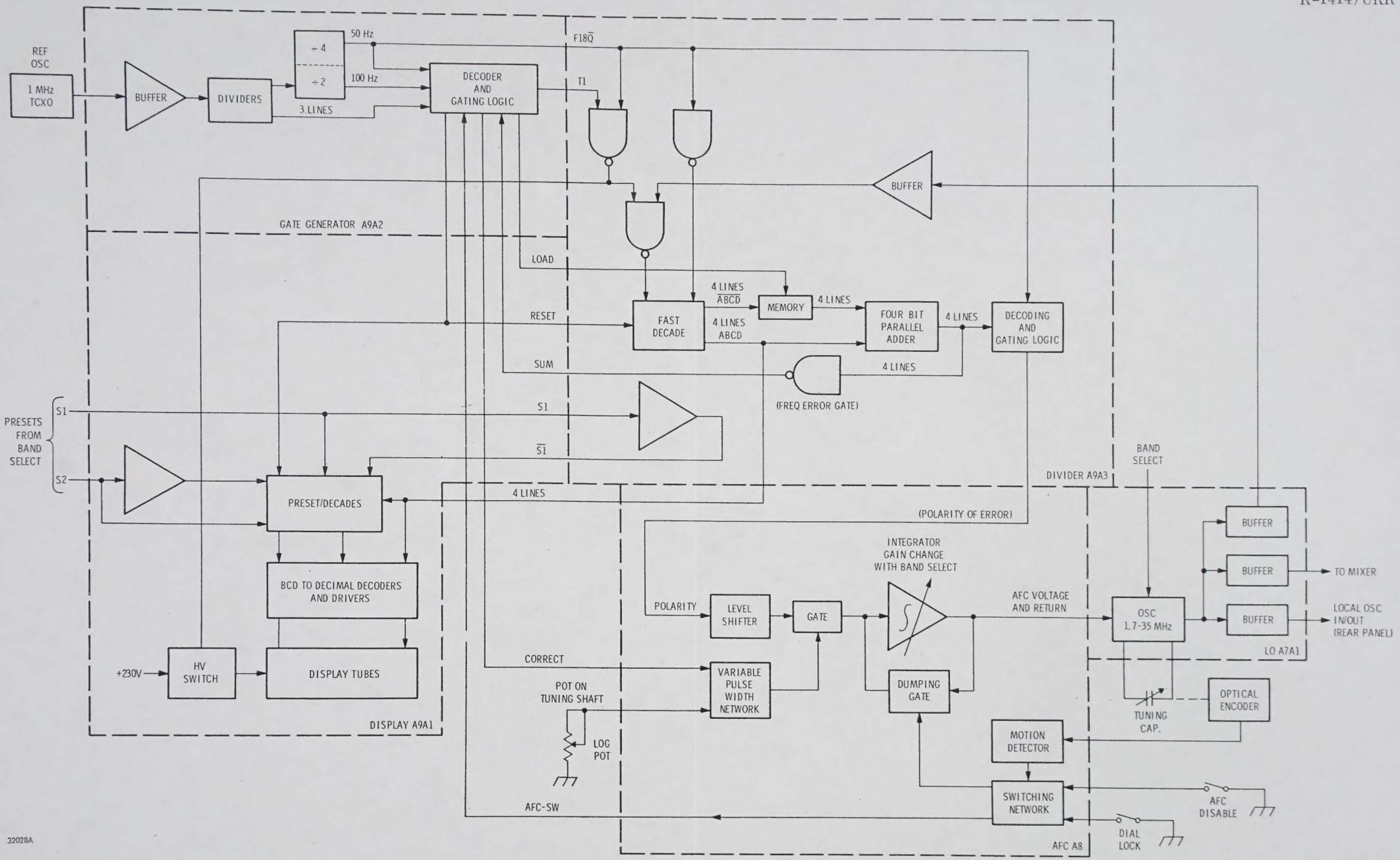


Figure 4-9. – AFC Loop and Counter, Block Diagram.

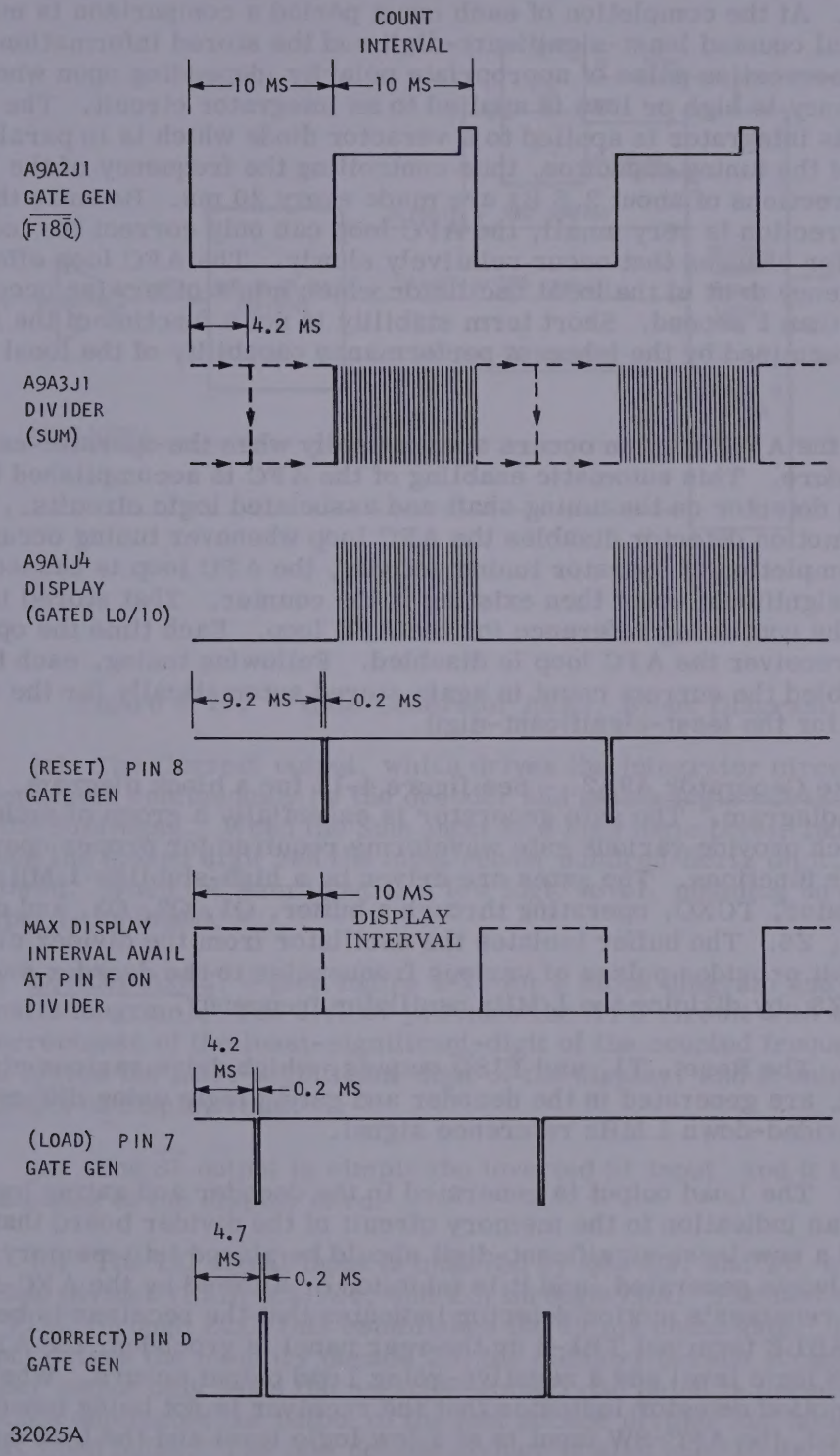


Figure 4-10. – Counter Timing Diagram.

is not related to any signal that may be present in the passband of the receiver. A digital storage register stores the information representing the desired least-significant-digit. At the completion of each count period a comparison is made between the actual counted least-significant-digit and the stored information. If an error exists, a correction pulse of appropriate polarity (depending upon whether the oscillator frequency is high or low) is applied to an integrator circuit. The DC output voltage of this integrator is applied to a varactor diode which is in parallel with the LO section of the tuning capacitor, thus controlling the frequency of the local oscillator. Corrections of about 3.5 Hz are made every 20 ms. Because the magnitude of the correction is very small, the AFC loop can only correct the local oscillator frequency for changes that occur relatively slowly. The AFC loop effectively eliminates frequency drift of the local oscillator which might otherwise occur over periods greater than 1 second. Short term stability is not a function of the AFC loop, but rather is determined by the inherent performance capability of the local oscillator circuit.

Enabling of the AFC function occurs automatically when the operator completes his tuning procudure. This automatic enabling of the AFC is accomplished by a sensitive motion detector on the tuning shaft and associated logic circuits. The electro-optical motion detector disables the AFC loop whenever tuning occurs. Following the completion of operator tuning activity, the AFC loop is caused to store the actual least significant count then existing in the counter. That stored information is used as the continuing reference for the AFC loop. Each time the operator again tunes the receiver the AFC loop is disabled. Following tuning, each time the AFC loop is enabled the current count is again stored automatically for the new reference value for the least-significant-digit.

(1) Gate Generator A9A2. - See figure 4-11 for a block diagram, figure A-13 for a schematic diagram. The gate generator is essentially a group of multi-input NAND gates which provide various gate waveforms required for proper operation of all of the counter functions. The gates are driven by a high-stability 1 MHz crystal reference oscillator, TCXO, operating through a buffer, Q1, Q2, Q3, and dividers, Z1, Z2, Z3, Z4, Z5. The buffer isolates the oscillator from the divider circuit, and the divider circuit provides pulses of various frequencies to the decoder and gating logic, Z6, Z7, Z8, by dividing the 1 MHz oscillator frequency.

(a) The Reset, T1, and F18$\overline{Q}$ outputs, which drive various circuits on the divider card, are generated in the decoder and gating logic using different combinations of the divided-down 1 MHz reference signal.

(b) The Load output is generated in the decoder and gating logic and is used to provide an indication to the memory circuit of the divider board that the AFC is disabled, and a new least-significant-digit should be placed into memory. The Load output is always generated, and it is inhibited or allowed by the AFC-SW input. When either the receiver's motion detector indicates that the receiver is being tuned or the AFC DISABLE terminal TB1-3 on the rear panel is grounded, the AFC-SW input is at a high logic level and a negative-going Load output occurs. When either the receiver's motion detector indicates that the receiver is not being tuned or the dial lock is locked, the AFC-SW input is at a low logic level and the load output is inhibited.

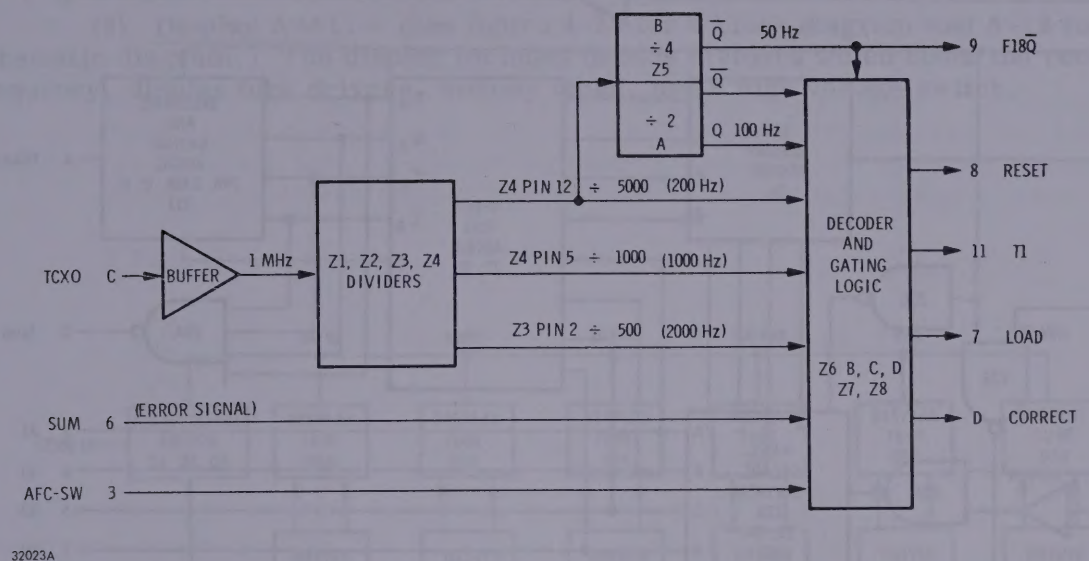


Figure 4-11. – Gate Generator A9A2, Block Diagram.

(c) The Correct output, which drives the integrator circuit on the AFC board, is generated continuously by the decoder and gating logic but is inhibited or allowed by the Sum input. When the Sum input is a high logic level, indicating an error between the stored digit and the most recent hundred-hertz digit, a Correct pulse is allowed. When the Sum input is a low logic level, meaning no error, the Correct output is inhibited.

(2) Divider A9A3. - (See figure 4-12 for a block diagram and figure A-14 for a schematic diagram.) The divider provides the AFC circuit with information about the correctness of the least-significant-digit of the counted frequency. The divider also drives the least-significant-digit of the display, and it determines the maximum length of display time.

(a) The $\overline{S1}$ output is simply the inverted S1 input, and it is used to preset the decades in the display card.

(b) The LO signal input is buffered by Q1, Q2, and Z1, and gated into the fast decade divider (Z2D, Z3, Z4, and Z5) through Z2A. The fast decade divider is gated by F18$\overline{Q}$ through Z2C; this establishes the 10 ms count gate. The fast decade divider output drives the memory decade Z6; the memory decade accepts the fast decade divider output only when the negative-going Load pulse is present. The memory decade duplicates the output of the fast decade divider and holds this output until the next Load pulse. The fast decade divider is also used to drive the hundred-cycle digit of the display and also the 4-bit full adder, Z7 and Z8, which determines whether or not an error is present between the stored digit and the hundred-cycle digit.

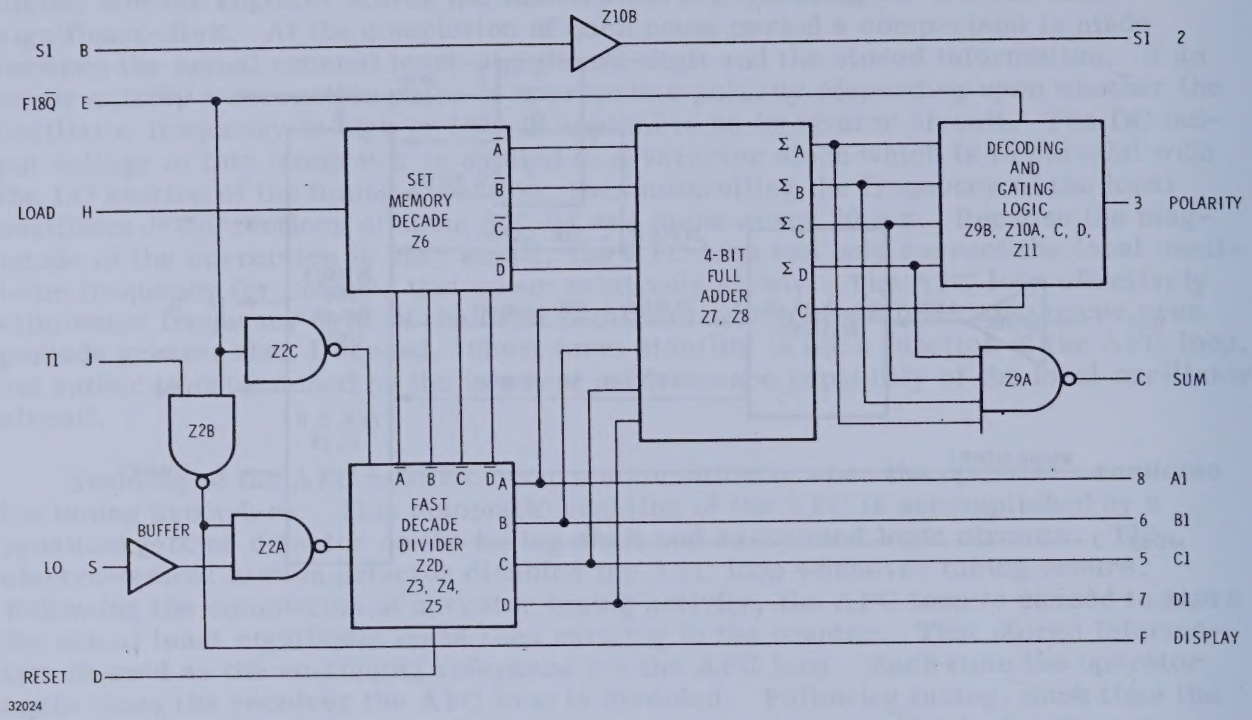


Figure 4-12. – Divider A9A3, Block Diagram.

(c) The Sum output, which indicates to the AFC circuit whether or not an error exists between the stored digit and the hundred-cycle digit, is a result of the Σ_A, Σ_B, Σ_C, and Σ_D outputs of the 4-bit full adder, Z7 and Z8. If all of the full adder outputs are high, indicating no error between the stored digit and the hundred-cycle digit, the Sum output is at a low logic level. If any one or more of the full adder outputs are low, meaning an error between the stored digit and the hundred-cycle digit, the Sum output is at a high logic level.

(d) The Polarity output is a function of the sum (Σ_A, Σ_B, Σ_C, Σ_D) and carry (C) outputs of the 4-bit full adder and is gated by the 50 Hz basic count rate (F18$\overline{Q}$) through Z11B. The necessary logic is performed by the decoding and gating logic circuit, Z9B, Z10, and Z11. When the hundred-cycle digit of the last count is greater than the stored digit by 1, 2, 3, or 4, the Polarity output is at the high logic level. When the hundred-cycle digit of the last count is equal to or less than the stored digit by 1, 2, 3, 4, or 5, the Polarity output is at the low logic level.

(e) When the hundred-cycle digit of the last count falls outside of the limits defined above, the AFC loop corrects to the next thousand-cycle digit. For example, when the hundred-cycle digit of the last count is less than the stored digit by 6, the Polarity output indicates that the hundred-cycle digit of the last count is greater than the stored digit by 4. Therefore, the AFC lock is lost and the AFC loop jumps to the next kilocycle digit.

(f) The Display output, which triggers the high voltage switch on the Display board and determines the display pulse width, is gated by the T1 input through Z3B. (See also the timing diagram, figure 4-10.) The T1 input is used to shorten

the Display output to 9 ms (it would be 10 msec otherwise) and during the last 1 ms of T1 input the Reset pulse arrives resetting the fast decade divider.

(3) Display A9A1. - (See figure 4-13 for a block diagram and A-12 for a schematic diagram.) The display includes decade dividers which count the receiver frequency, display tube drivers, display tubes, and a high voltage switch.

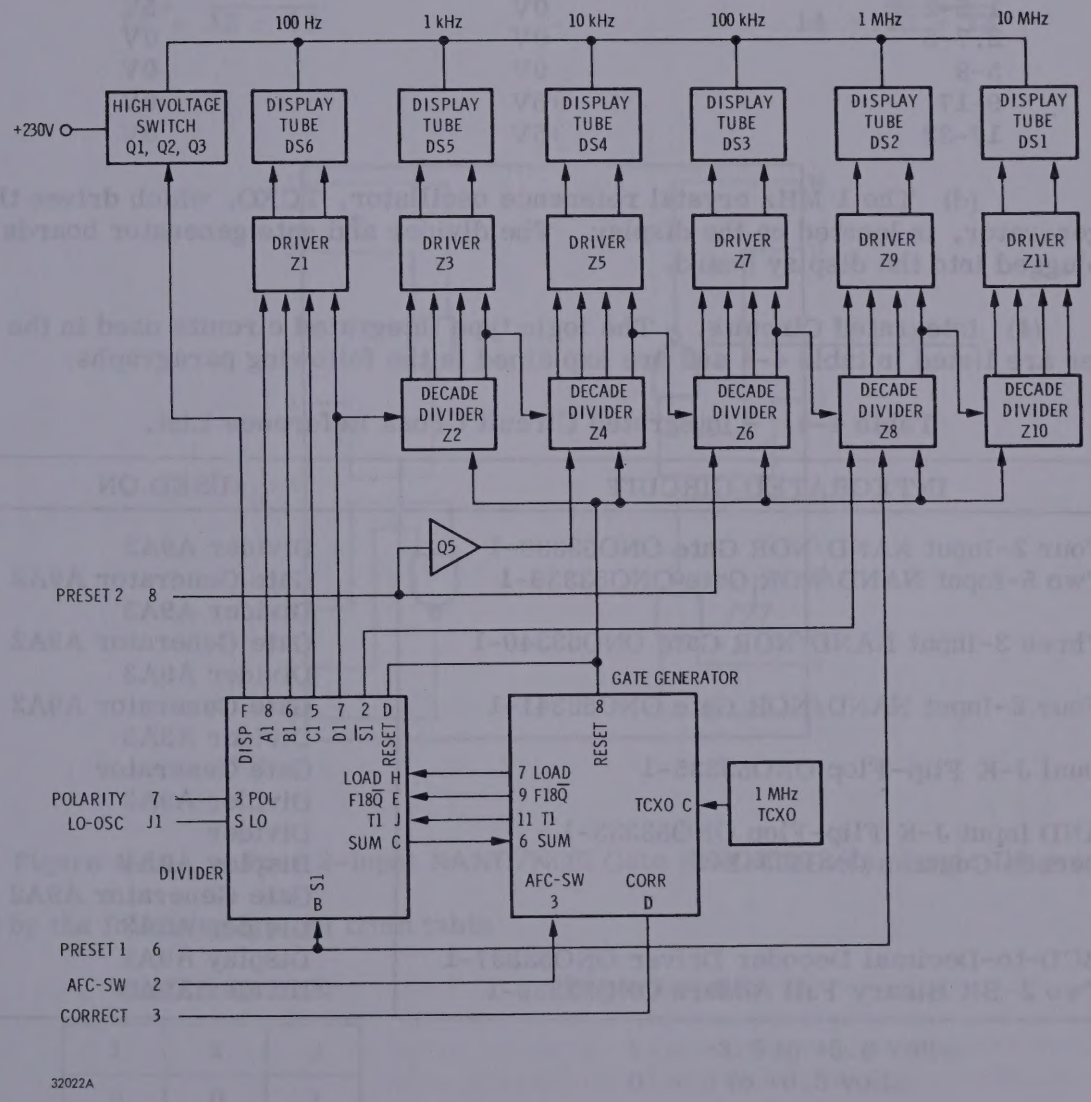


Figure 4-13. – Display A9A1, Block Diagram.

(a) The fast decade divider on the divider card drives the display tube driver, Z1, for the hundred-cycle (least-significant) digit. The other display tube drivers are operated by decade dividers which count the receiver frequency.

(b) The high voltage switch Q1, Q2, Q3, which controls the high voltage to the display tubes, is triggered by the Display output of the divider card. The pulse width of 10 msec is determined by the Display signal; therefore, the duty cycle is 50 percent. (See also the timing diagram, figure 4-10.)

(c) The Reset input from the gate generator resets all of the decades simultaneously. The decades must then be preset to the negative of the intermediate frequency, so that when the counter reads the LO frequency the IF is subtracted, and the frequency to which the receiver is tuned is displayed. The preset is controlled by the Preset 1 and Preset 2 inputs from the BAND-MHZ switch as follows:

BAND-MHZ	Preset 1	Preset 2
1.5-2.7	0V	+5V
2.7-5	0V	0V
5-9	0V	0V
9-17	+5V	0V
17-32	+5V	0V

(d) The 1 MHz crystal reference oscillator, TCXO, which drives the gate generator, is located on the display. The divider and gate generator boards are also plugged into the display board.

(4) Integrated Circuits. - The logic type integrated circuits used in the counter are listed in table 4-4 and are explained in the following paragraphs.

Table 4-4. – Integrated Circuit Cross Reference List.

INTEGRATED CIRCUIT	USED ON
Four 2-Input NAND/NOR Gate ONO53338-1	Divider A9A3
Two 5-Input NAND/NOR Gate ONO53339-1	Gate Generator A9A2
	Divider A9A3
Three 3-Input NAND/NOR Gate ONO53340-1	Gate Generator A9A2
	Divider A9A3
Four 2-Input NAND/NOR Gate ONO53341-1	Gate Generator A9A2
	Divider A9A3
Dual J-K Flip-Flop ONO53335-1	Gate Generator
	Divider A9A3
AND Input J-K Flip-Flop ONO53333-1	Divider
Decade Counter ONO53342-1	Display A9A1
	Gate Generator A9A2
	Divider A9A3
BCD-to-Decimal Decoder Driver ONO53337-1	Display A9A1
Two 2-Bit Binary Full Adders ONO53336-1	Divider A9A3

(a) The four 2-input NAND/NOR gate (ONO53338-1) integrated circuit consists of four 2-input gates. Each gate functions as a NAND-gate in positive logic and as a NOR-gate in negative logic. Figure 4-14 provides a logic diagram of the circuit. The operation of the gates are described by the following logic equations:

(+) Logic	(-) Logic
$3 = \overline{1 \cdot 2}$	$3 = \overline{1 + 2}$
$7 = \overline{5 \cdot 6}$	$7 = \overline{5 + 6}$
$11 = \overline{8 \cdot 9}$	$11 = \overline{8 + 9}$
$14 = \overline{12 \cdot 13}$	$14 = \overline{12 + 13}$

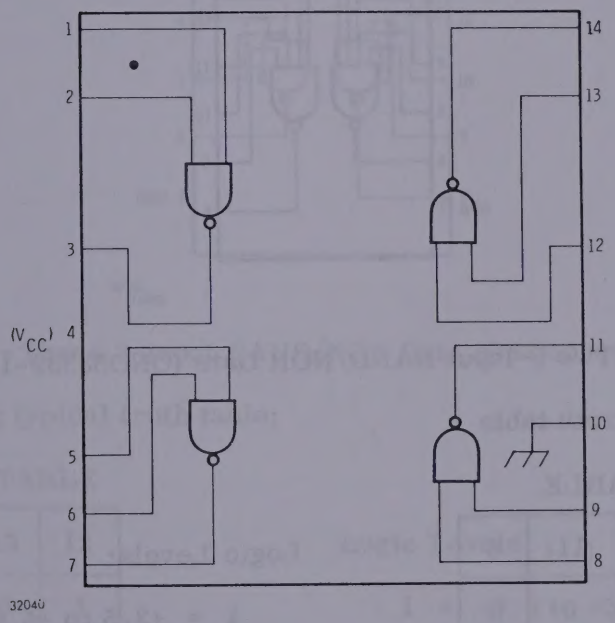


Figure 4-14. – Four 2-Input NAND/NOR Gate (ONO53338-1), Logic Diagram.

and by the following typical truth table

TRUTH TABLE

1	2	3
0	0	1
0	1	1
1	0	1
1	1	0

Logic Levels:

1 = +3.5 to +5.0 volts
0 = 0 to +0.5 volts

(b) The two 5-input NAND/NOR gate (ONO53339-1) integrated circuit consists of two 5-input gates. Each gate functions as a NAND-gate in positive logic and as a NOR-gate in negative logic. Figure 4-15 provides a logic diagram of the circuit. The operation of the gates are described by the following logic equations:

(+) Logic	(-) Logic
$6 = \overline{1 \cdot 2 \cdot 4 \cdot 5 \cdot (3)}$	$6 = \overline{1 + 2 + 4 + 5 + (3)}$
$8 = \overline{9 \cdot 10 \cdot 12 \cdot 13 \cdot (11)}$	$8 = \overline{9 + 10 + 12 + 13 + (11)}$

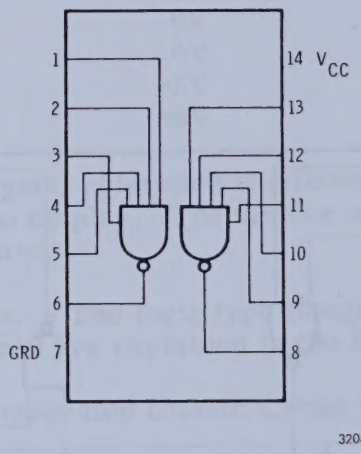


Figure 4-15. – Two 5-Input NAND/NOR Gate (ONO53339-1), Logic Diagram.

and by the following truth table

TRUTH TABLE

1	2	4	5	(11)	6
0	0	0	0	0	0
0	0	0	0	1	1
1	1	1	1	0	1
1	1	1	1	1	0

Logic Levels:

1 = +3.5 to +5.0 volts
0 = 0 to +0.5 volt

(c) The three 3-input NAND/NOR gate (ONO53340-1) integrated circuit consists of three 3-input gates. Each gate functions as a NAND-gate in positive logic and as a NOR-gate in negative logic. Figure 4-16 provides a logic diagram of the circuit. The operation of the gates are described by the following logic equations:

(+) Logic

$12 = \overline{1 \cdot 2 \cdot 13}$

$6 = \overline{3 \cdot 4 \cdot 5}$

$8 = \overline{9 \cdot 10 \cdot 11}$

(-) Logic

$12 = \overline{1 + 2 + 13}$

$6 = \overline{3 + 4 + 5}$

$8 = \overline{9 + 10 + 11}$

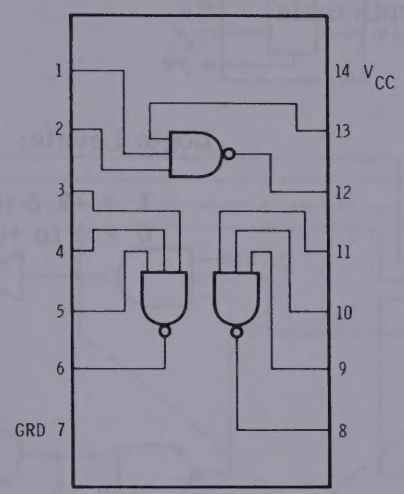


Figure 4-16. – Three 3-Input NAND/NOR Gate (ONO53340-1), Logic Diagram.

and by the following typical truth table:

TRUTH TABLE

1	2	13	12
0	0	0	1
0	0	1	1
1	1	0	1
1	1	1	0

Logic Levels:

1 = +3.5 to +5.0 volts
0 = 0 to +0.5 volt

(d) The four 2-input NAND/NOR gate (ONO53341-1) integrated circuit consists of four 2-input gates. Each gate functions as a NAND-gate in positive logic and as a NOR-gate in negative logic. Figure 4-17 provides a logic diagram of the circuit. The operation of the gates are described by the following logic equations:

(+) Logic	(-) Logic
$3 = \overline{1 \cdot 2}$	$3 = \overline{1 + 2}$
$6 = \overline{4 \cdot 5}$	$6 = \overline{4 + 5}$
$8 = \overline{9 \cdot 10}$	$8 = \overline{9 + 10}$
$11 = \overline{12 \cdot 13}$	$11 = \overline{12 + 13}$

and by the following typical truth table:

TRUTH TABLE		
1	2	3
0	0	1
0	1	1
1	0	1
1	1	0

Logic Levels:

1 = +3.5 to +5.0 volts
0 = 0 to +0.5 volt

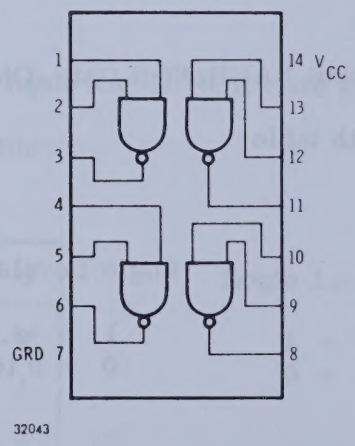


Figure 4-17. – Four 2-Input NAND/NOR Gates (ONO53341-1), Logic Diagram.

(e) The dual J-K flip-flop (ONO53335-1) integrated circuit consists of two J-K flip-flops with a common clock input. Figure 4-18 provides a logic diagram of the circuit. The operation of each flip-flop is described by the following equations:

$$Q_n{+}1 \text{ (set)} = J\overline{Q}_n + K\overline{Q}_n$$

$$\overline{Q}_n{+}1 \text{ (reset)} = \overline{J}Q_n + KQ_n$$

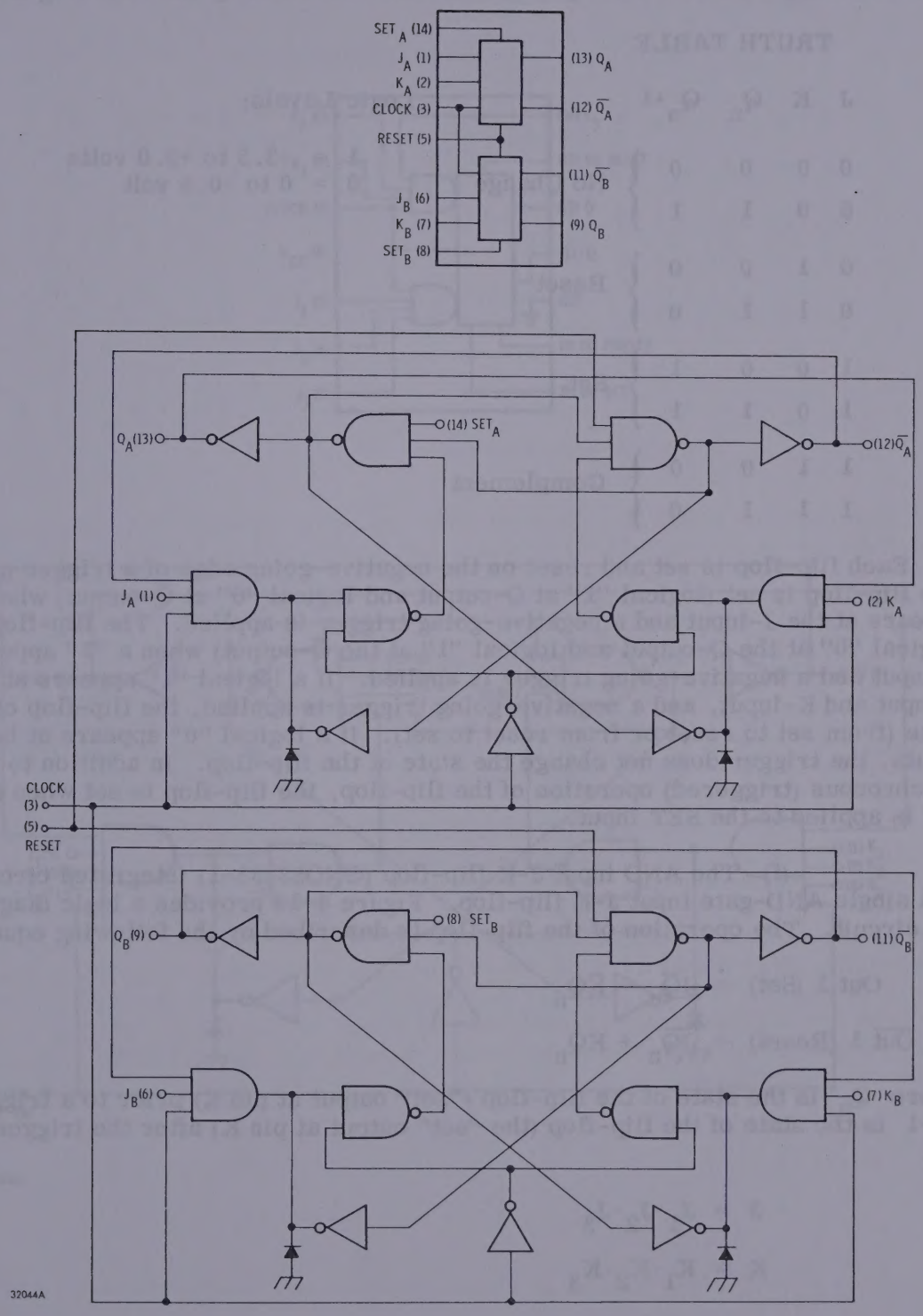


Figure 4-18. – Dual J-K Flip-Flop (ONO53335-1), Logic Diagram.

where Q_n is the state of the flip-flop (the "set" outputs at pins 9 and 12) prior to the trigger pulse, Q_n+1 is the state of the flip-flop (the set outputs at pins 11 and 12) after the trigger pulse. The operation is also described by the following truth table:

TRUTH TABLE

J	K	Q_n	Q_n+1	
0	0	0	0	No Change
0	0	1	1	
0	1	0	0	Reset
0	1	1	0	
1	0	0	1	Set
1	0	1	1	
1	1	0	0	Complement
1	1	1	0	

Logic Levels:

1 = +3.5 to +5.0 volts
0 = 0 to +0.5 volt

Each flip-flop is set and reset on the negative-going edge of a trigger pulse. The flip-flop is set (logical "1" at Q-output and logical "0" at $\overline{Q}$-output) when a "1" appears at the J-input and a negative-going trigger is applied. The flip-flop is reset (logical "0" at the Q-output and logical "1" at the $\overline{Q}$-output) when a "1" appears at the K-input and a negative-going trigger is applied. If a logical "1" appears at both the J-input and K-input, and a negative-going trigger is applied, the flip-flop changes state (from set to reset or from reset to set). If a logical "0" appears at both the inputs, the trigger does not change the state of the flip-flop. In addition to the synchronous (triggered) operation of the flip-flop, the flip-flop is set when a logical "0" is applied to the SET input.

(f) The AND input J-K flip-flop (ONO53333-1) integrated circuit consists of a single AND-gate input J-K flip-flop. Figure 4-19 provides a logic diagram of the circuit. The operation of the flip-flop is described by the following equations:

$$\text{Out 1 (Set)} = J\overline{Q}_n + \overline{K}Q_n$$

$$\overline{\text{Out 1}}\ \text{(Reset)} = \overline{J}\overline{Q}_n + KQ_n$$

where Q_n is the state of the flip-flop ("set" output at pin K) prior to a trigger pulse, Q_n+1 is the state of the flip-flop (the "set" output at pin K) after the trigger pulse, and

$$J = J_1 \cdot J_2 \cdot J_3$$

$$K = K_1 \cdot K_2 \cdot K_3$$

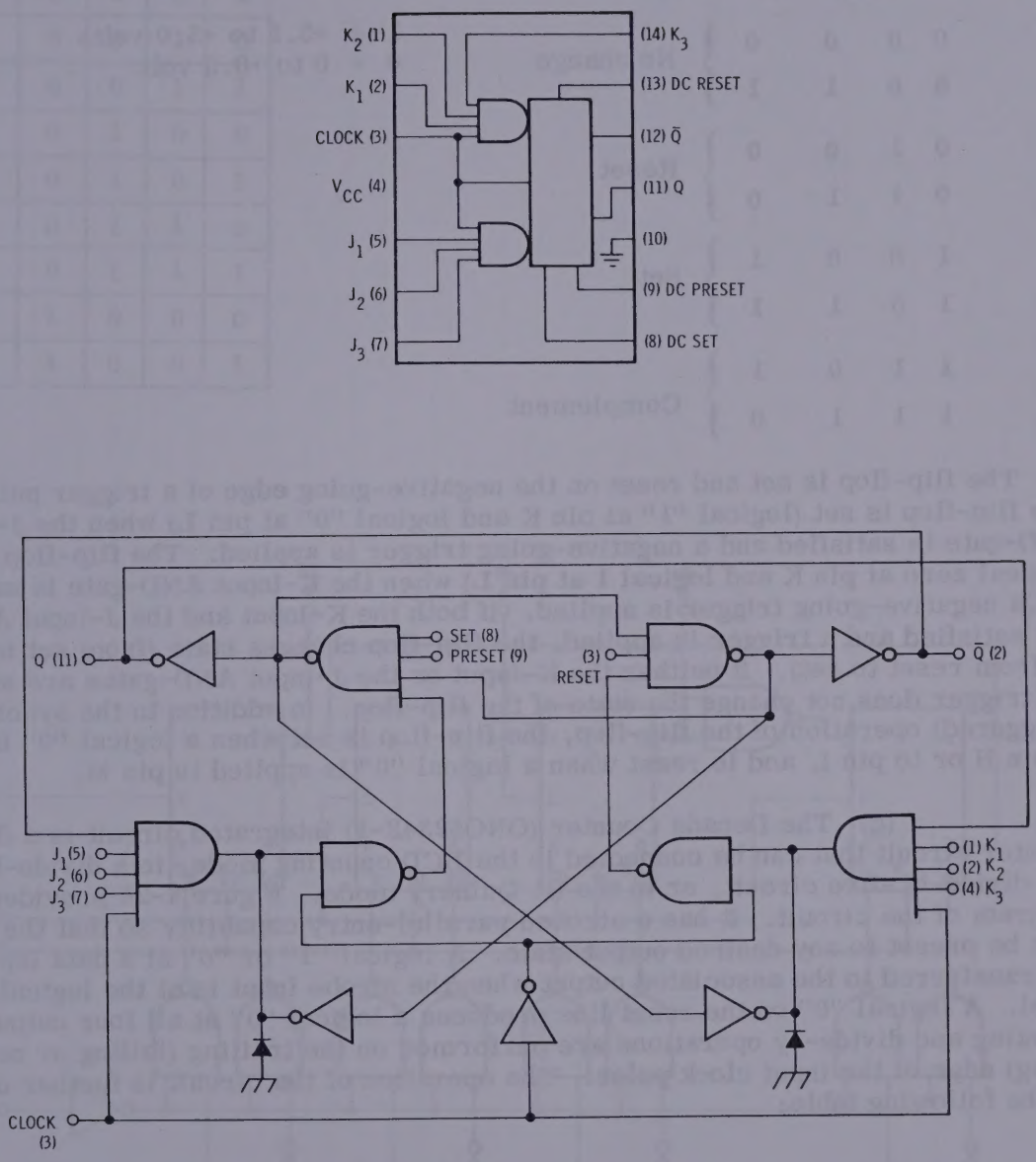


Figure 4-19. – AND Input J-K Flip-Flop (ONO53333-1), Logic Diagram.

The operation is also described by the following truth table:

TRUTH TABLE

J	K	Q_n	Q_n+1	
0	0	0	0	No change
0	0	1	1	
0	1	0	0	Reset
0	1	1	0	
1	0	0	1	Set
1	0	1	1	
1	1	0	1	Complement
1	1	1	0	

Logic Levels:

1 = +3.5 to +5.0 volts
0 = 0 to +0.5 volt

The flip-flop is set and reset on the negative-going edge of a trigger pulse. The flip-flop is set (logical "1" at pin K and logical "0" at pin L) when the J-input AND-gate is satisfied and a negative-going trigger is applied. The flip-flop is reset (logical zero at pin K and logical 1 at pin L) when the K-input AND-gate is satisfied and a negative-going trigger is applied. If both the K-input and the J-input AND-gates are satisfied and a trigger is applied, the flip-flop changes state (from set to reset, or from reset to set). If neither the K-input or the J-input AND-gates are satisfied, the trigger does not change the state of the flip-flop. In addition to the synchronous (triggered) operation of the flip-flop, the flip-flop is set when a logical "0" is applied to pin H or to pin I, and is reset when a logical "0" is applied to pin M.

(g) The Decade Counter (ONO53342-1) integrated circuit is a decade counter circuit that can be connected in the BCD counting mode, in a divide-by-two and divide-by-five circuit, or in the Bi-Quinary mode. Figure 4-20 provides a logic diagram of the circuit. It has a strobed parallel-entry capability so that the counter may be preset to any desired output state. A logical "1" or "0" at a data input will be transferred to the associated output when the strobe input is at the logical "0" level. A logical "0" on the reset line produces a logical "0" at all four outputs. The counting and divide-by operations are performed on the trailing (falling or negative-going) edge of the input clock pulse. The operation of the circuit is further described by the following table:

INPUT PULSES	OUTPUTS			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Logic Levels:

0 = 0 to +0.5 volt
1 = +3.5 to +5.0 volts

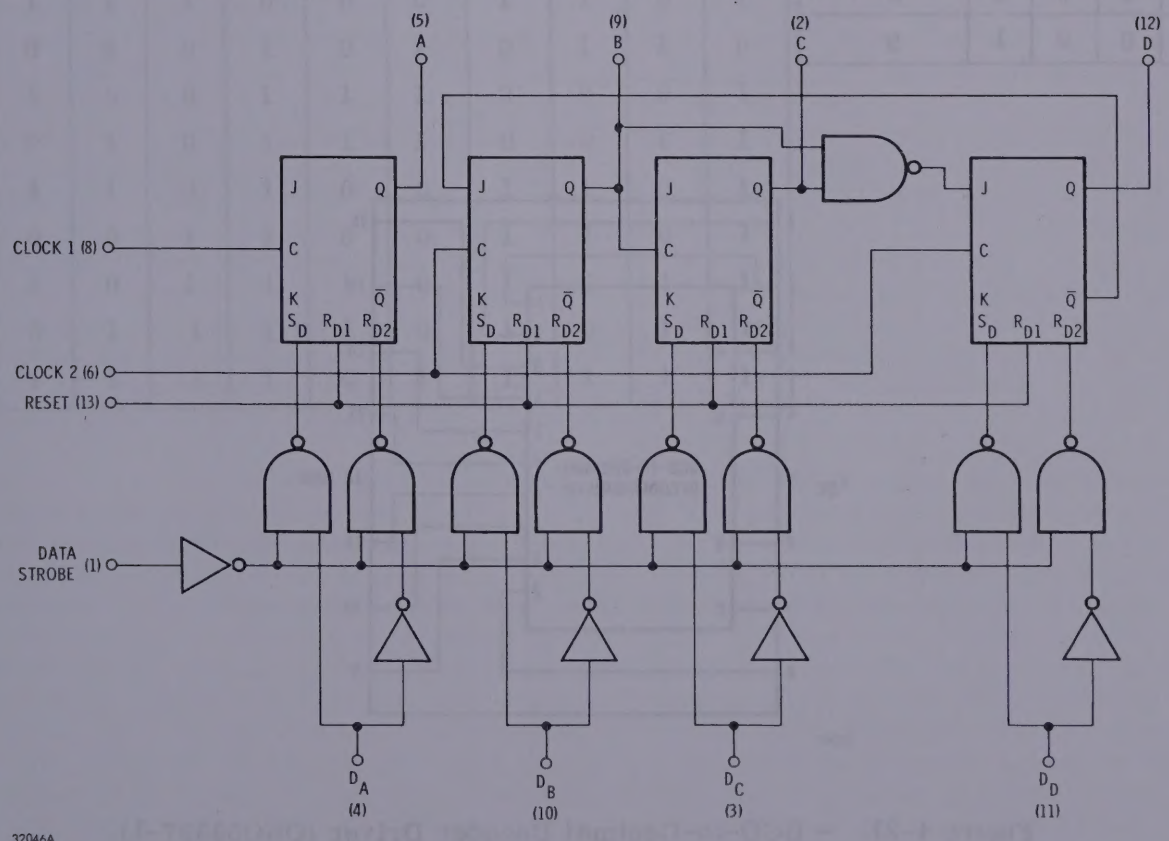


Figure 4-20. – Decade Counter (ONO53342-1), Logic Diagram.

(h) The BCD-to-decimal decoder driver (ONO53337-1) integrated circuit is a BCD-to-decimal decoder designed to drive indicator tubes. It consists of transistor-transistor logic (TTL) gate circuits which select one of ten decimal output drivers. Refer to figure 4-21 for a logic diagram of the circuit. The operation of the circuit is described by the following table:

TRUTH TABLE

INPUTS				OUTPUT
D	C	B	A	ON
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

NOTES:

1. Input logic levels

   0 = 0 to +0.5 volt
   1 = +3.5 to +5 volts

2. Output levels

   ON = GND
   OFF = OPEN CIRCUIT

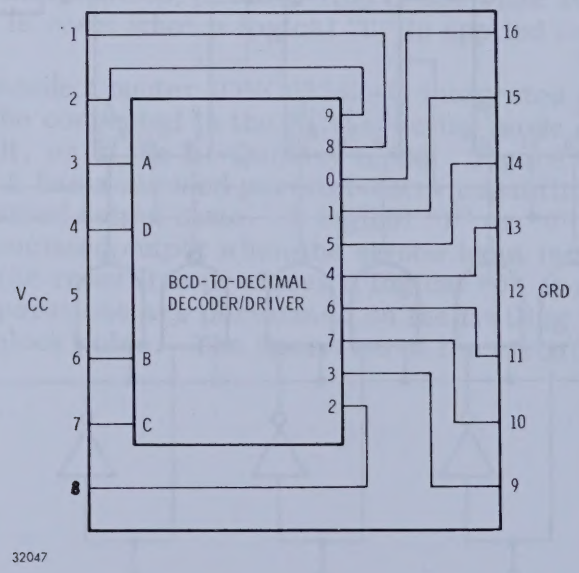


Figure 4-21. – BCD-to-Decimal Decoder Driver (ONO53337-1), Logic Diagram.

(i) The two 2-bit binary full adder (ONO53336-1) integrated circuit is used to perform the addition of two 2-bit binary numbers. Refer to figure 4-22 for a logic diagram of the circuit. The sum (Σ) outputs are provided for each bit and the resultant carry (C_2) is obtained from the second bit. The operation of the circuit is described by the following table:

INPUT				OUTPUT					
				WHEN $C_{in} = 0$			WHEN $C_{in} = 1$		
A_1	B_1	A_2	B_2	Σ_1	Σ_2	C_2	Σ_1	Σ_2	C_2
0	0	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0
1	1	0	0	0	1	0	1	1	0
0	0	1	0	0	1	0	1	1	0
1	0	1	0	1	1	0	0	0	1
0	1	1	0	1	1	0	0	0	1
1	1	1	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1	1	0
1	0	0	1	1	1	0	0	0	1
0	1	0	1	1	1	0	0	0	1
1	1	0	1	0	0	1	1	0	1
0	0	1	1	0	0	1	1	0	1
1	0	1	1	1	0	1	0	1	1
0	1	1	1	1	0	1	0	1	1
1	1	1	1	0	1	1	1	1	1

Logic Levels:

0 = 0 to +0.5 volt
1 = +3.5 to +5 volts

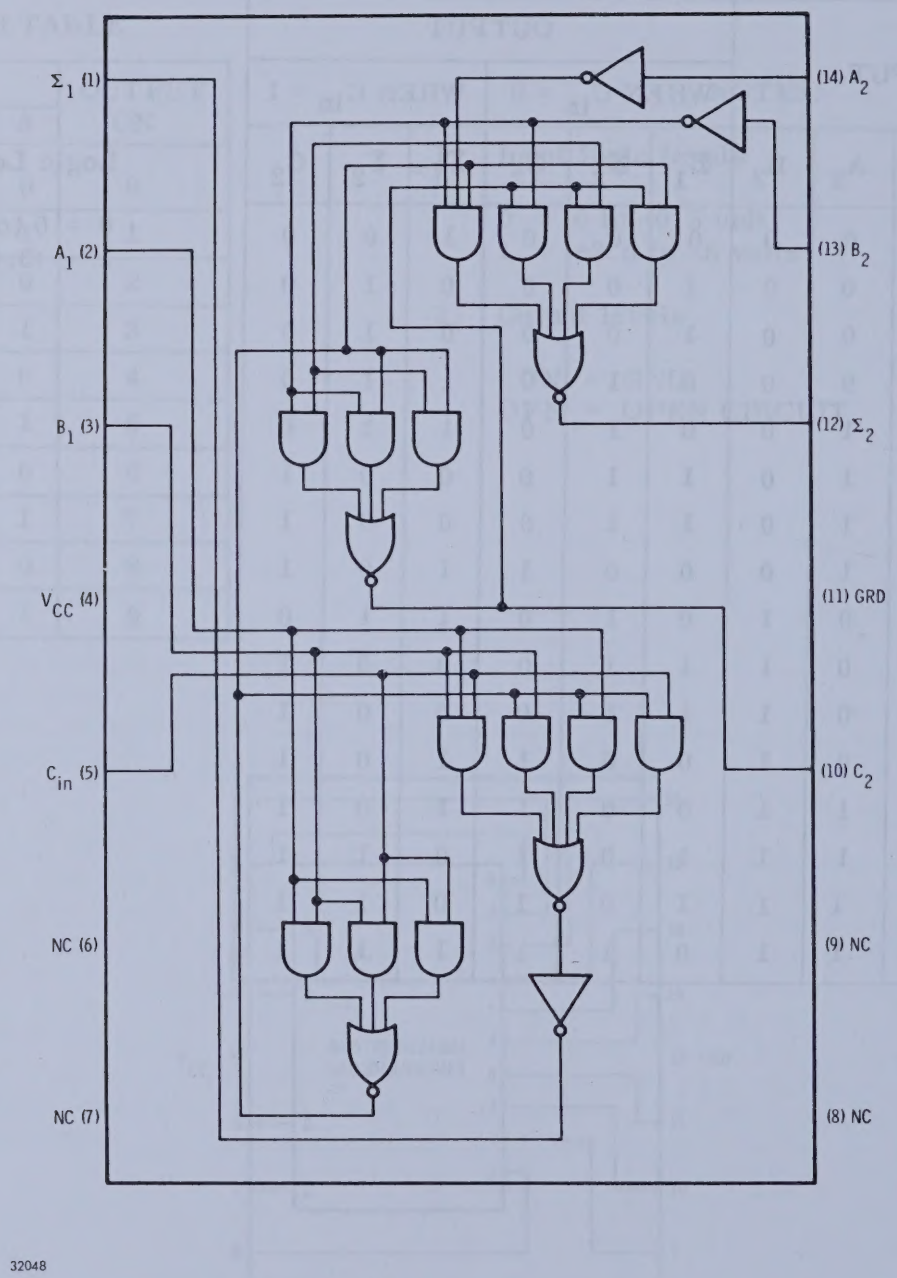


Figure 4-22. – 2-Bit Binary Full Adders (ONO53336-1), Logic Diagram.

(5) Automatic Frequency Control (AFC) A8. - (See figure 4-23 for a block diagram and A-15 for a schematic diagram.) The AFC works closely with the counter and frequency display to provide frequency correction information to the local oscillator, so that receiver drift is minimized.

(a) The Correct input from the divider drives the AFC gate, Q6, through a variable pulse width network, Q1, Q2, Q3. The variable pulse width network is operated by a logarithmic-taper potentiometer on the tuning shaft, since pulses of varying widths are needed in order to keep the amount of AFC frequency correction constant at about 3.5 Hz per Correct pulse. The output from the variable pulse width network enables the AFC gate to allow the level shifter output to drive the integrator input resistor. The level shifter, Q4, Q5 provides the appropriate level output to drive the integrator, depending upon the Polarity input and whether the LO frequency has to be increased or decreased. Since the sensitivity of the varicap controlling the frequency of the LO depends on the BAND-MHZ switch position, different integator input resistances must be used on each band to change the integrator gain and keep the frequency correction per Correct pulse constant at about 3.5 Hz. The integrator AR1, Q7, C10, uses an integrated circuit differential amplifier whose output is the AFC voltage applied to the varicap in the LO. The normal range of the AFC voltage is 0 to +20 volts.

(b) The AFC may be turned-off manually by grounding the AFC Ext Disable input to the switching network Q12, Q13, Q14, Q15. Locking the Dial Lock control freezes the AFC memory. However, provision has been made for automatic AFC control by means of the motion detector, which turns the AFC off while the receiver is being tuned and on when tuning has stopped. The phototransistor used in the motion detector drives the motion detector circuit, AR2, Q9, Q10, Q11, on the AFC board. The motion detector circuit determines whether or not the tuning knob is turning by noting any change in the phototransistor signal, indicating motion. If motion is noted, then the switching network, Q12, Q13, Q14, Q15, closes the dumping gate, which shorts the integrator feedback capacitor, C10. This stops integration and allows the receiver to be tuned freely. Once motion stops, the motion detector notes this and causes the switching network to open the dumping gate. This removes the short circuit from the feedback capacitor, and the AFC functions normally. Grounding the AFC Ext Disable shorts the feedback capacitor and turns the AFC off. With the AFC off, the AFC voltage is held constant at about 7.5 volts (near the varicap's mid-range).

(c) The performance of the AFC loop is much better than the 100 Hz least count resolution of the counter. This performance is accomplished because of the integrator in the loop and because the individual corrections are very small (typically about 3.5 Hz) compared to 100 Hz. Figure 4-24 shows the probability of a correct pulse being applied to the integrator circuit for various amounts of offset from the tuned frequency. As shown in the figure, if the frequency error is less than 100 Hz, then a correct pulse is not applied to the integrator during every count interval. The correction rate increases with increased frequency error until the frequency error reaches 100 Hz or more, where the correction rate remains constant at one correct pulse per count interval. The correction rate becomes low as the tuned frequency is reached. However, if the frequency error is greater than -500 Hz or +400 Hz, the AFC lock is lost, and the receiver corrects toward the next kHz zone.

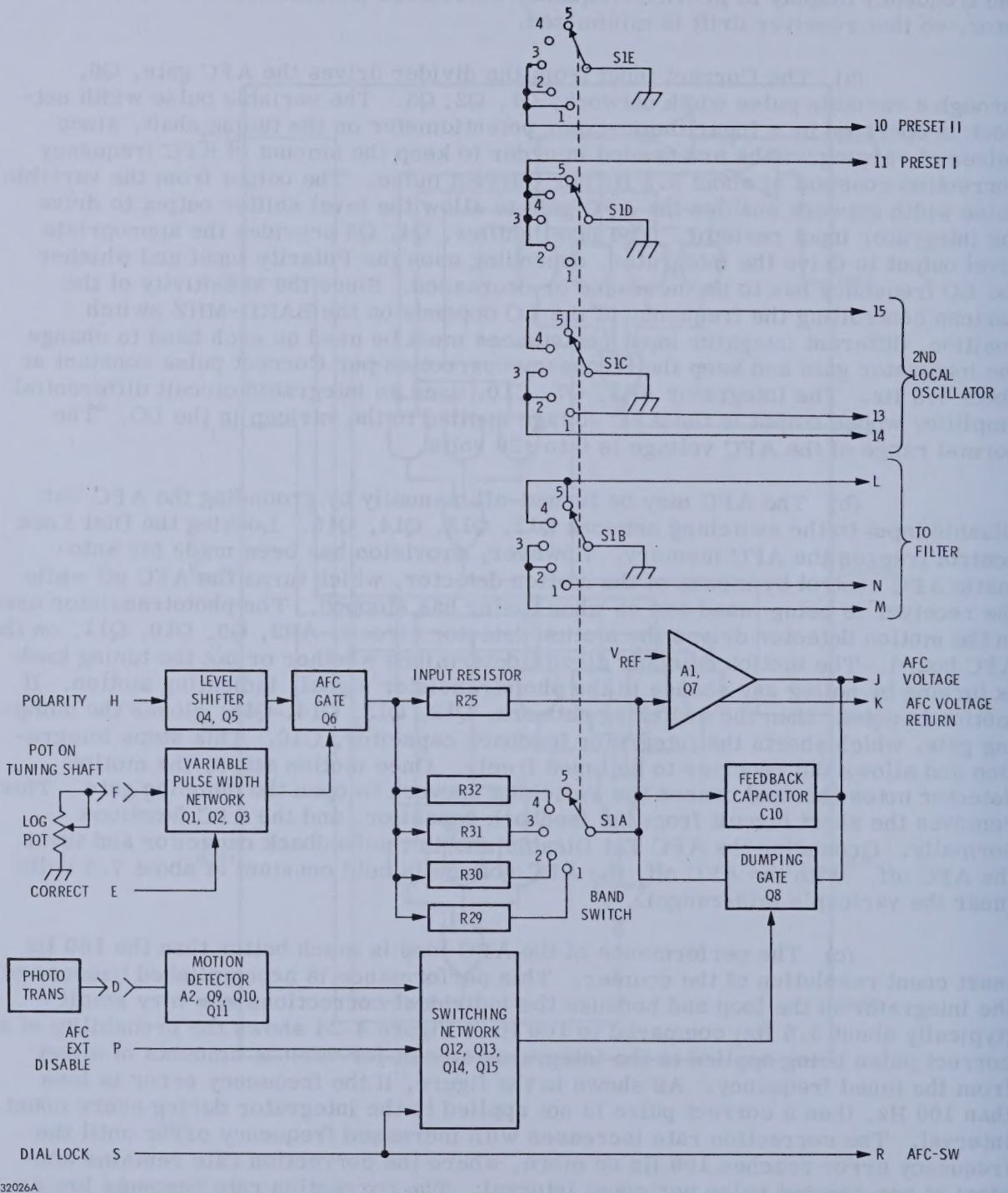


Figure 4-23. – Automatic Frequency Control (AFC) A8, Block Diagram.

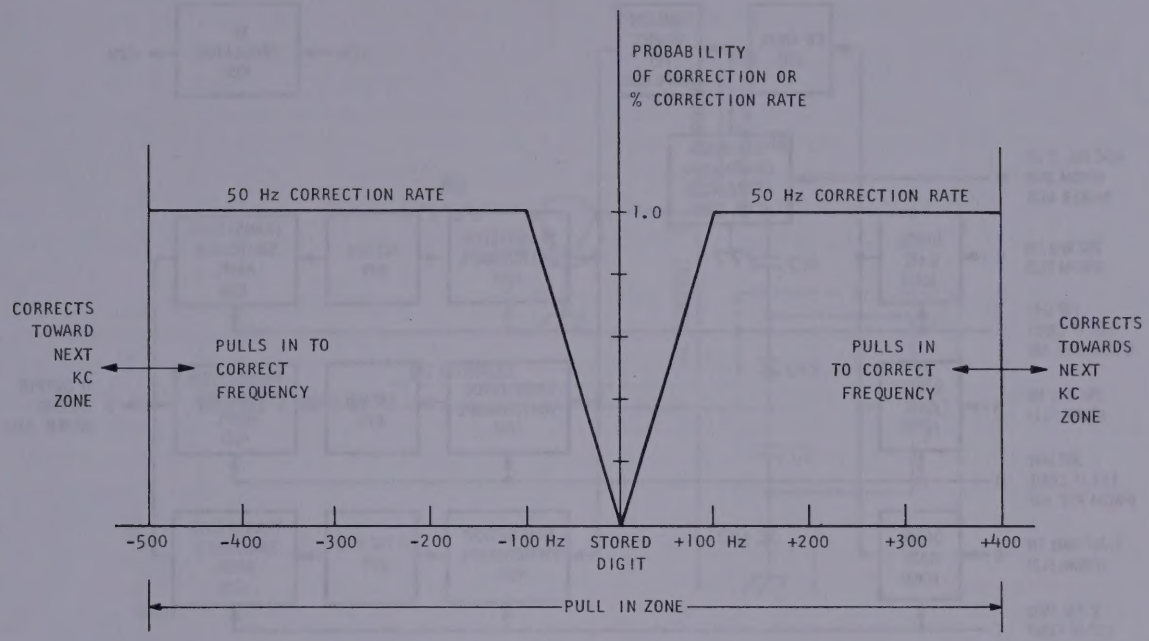


Figure 4-24. – AFC Loop Probability of Correction versus Frequency Error.

(d) It should be noted that during normal receiver operation the least significant digit of the display will occasionally indicate not only the stored digit, but also the next higher or next lower digit. This effect is normal, and it depends on the correction rate and probability of correction.

(e) Switch S1 is part of BAND-MHZ switch that is controlled from the front panel of the receiver. This part of the BAND-MHZ switch has four functions. One section of the switch connects different size resistors in parallel with the input resistor R25 to the integrator. This changes the input resistance to the integrator for each BAND-MHZ switch position which changes the integrator gain and keeps the frequency correction per correct pulse constant at about 3.5 Hz. Another section of the switch provides ground potential outputs to the counter A9, first IF amplifier A10, and the second local oscillator A18. The ground preset outputs to the counter A9, preset the negative of the IF, so that when the counter reads the LO frequency the IF is subtracted and the receiver displays the frequency to which it is tuned. The ground outputs to the second LO select the three different crystal oscillator outputs. The ground outputs to the first IF amplifier select either the 0.392 MHz, 0.762 MHz, or the 2.762 MHz IF inputs for further amplification.

i. First IF Amplier A10. - (See figure 4-25 for a block diagram and figure A-16 for a schematic diagram.) The first IF amplifier consists basically of IF amplifiers, switching circuits for connecting one of three IF inputs through amplifier circuits, and a band-pass filter. An AGC input is also available for automatically controlling the amplifier gain.

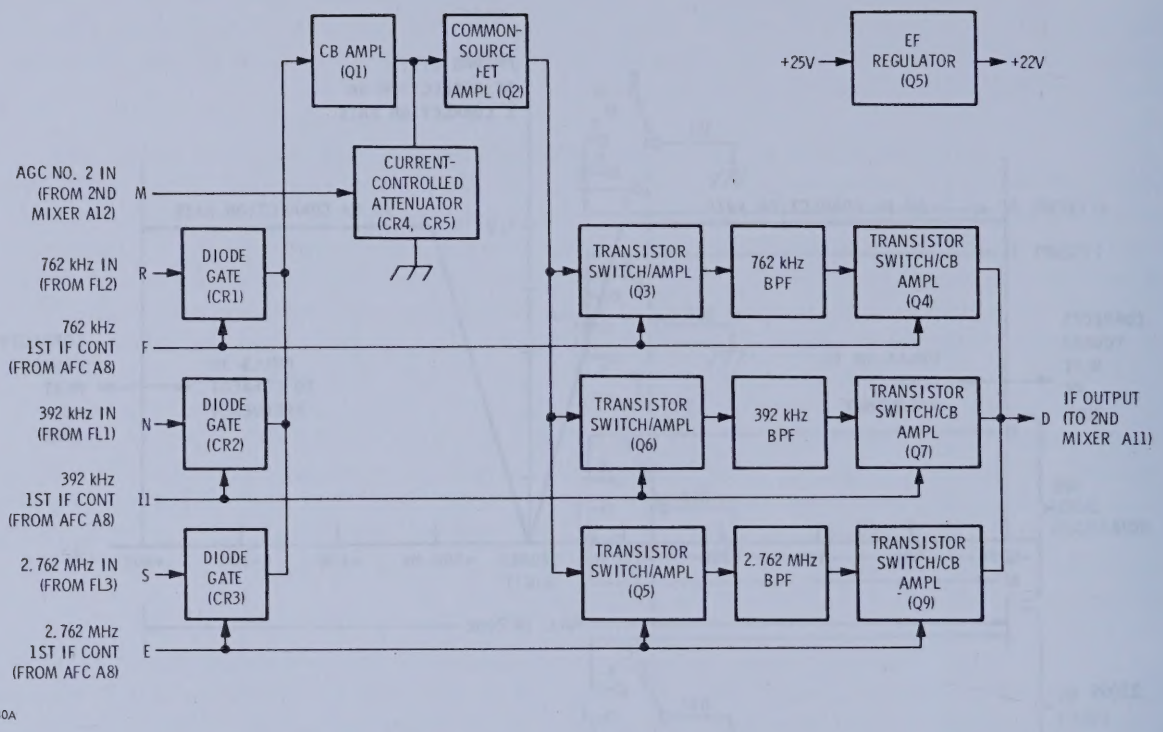


Figure 4-25. – First IF Amplifier A10, Block Diagram.

(1) Diode Gate Circuits. - The gate circuits for the 762 kHz, 392 kHz, and 2.762 MHz inputs are identical in operation, therefore, only one gate circuit will be explained. Diode CR1 is in series between the 762 kHz IF input at pin R and the input resistor R10 of the common-base amplifier Q1. When the 762 kHz control at pin F is open-circuited, diode CR1 will be back-biased. When CR1 is back-biased, the gate is open. When pin F is grounded, the emitter current of Q1 flows through R10, CR1, R2, L1, and R1; forward-biasing CR1. With CR1 forward biased, the gate is closed and the 762 kHz input is applied to the common-base amplifier Q1.

(2) Current-Controlled Attenuator. - The AGC No. 2 input from a current source in the second mixer A11 is coupled in at pin M. Increasing the dc input current increases the forward biasing of diodes CR4 and CR5 of the current-controlled attenuator. (See figure 4-26.) This causes their dynamic resistance to decrease. The dynamic resistance of the diodes is in parallel with the collector resistance R14 of Q1. Therefore, the gain of Q1 decreases for increasing input dc current at the AGC No. 2 input at pin M.

(3) IF Amplifiers. - The selected IF output of Q1 is further amplified by common-source FET amplifier Q2. The output of Q2 is coupled to the inputs of three transistor switch-amplifiers Q3, Q6, and Q8. The transistor switch circuits of Q3, Q6, and Q8 are identical so only Q3 will be discussed. Transistor switch-amplifier Q3, along with Q4, is controlled by the same IF control circuit that operates the input diode gate. When pin F is open-circuited, switch-amplifier Q3 is turned off and introduces a high loss between the FET amplifier Q2 and the 762 kHz band-pass filter. Switch-amplifier Q4 is also turned off which provides a high loss between the 762 kHz

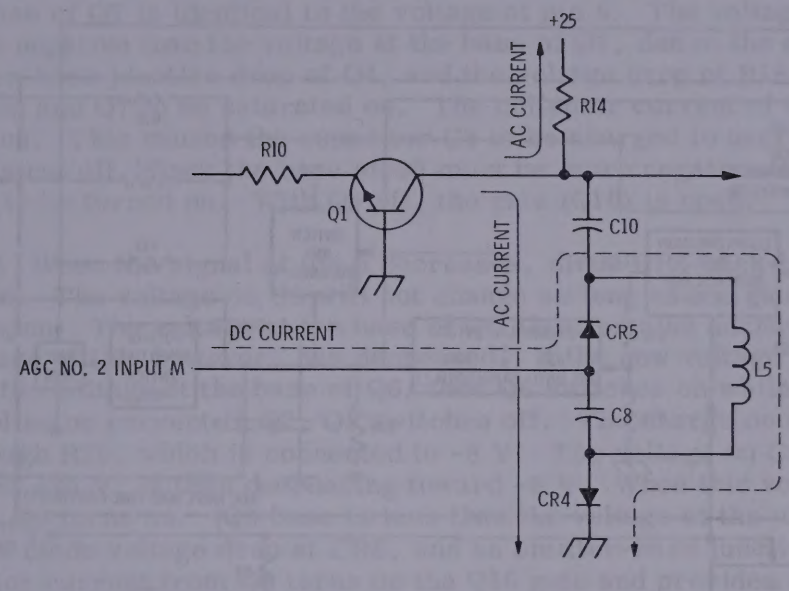


Figure 4-26. – Current-Controlled Attenuator.

band-pass filter and the output pin D. When pin F is grounded, transistor switch-amplifiers Q3 and Q4 are biased-on, coupling the 762 kHz IF signal through the band-pass filter to the output pin D. Only one of the three IF signals 762 kHz, 392 kHz, and 2.762 MHz is coupled through to the output pin D at any one time.

(4) Voltage-Regulator. - The emitter-follower regulator Q5 filters the ac variations from the +25 vdc power input to the remaining circuits on the first IF amplifier board.

j. Second Mixer A11. - (See figure 4-27 for a block diagram and figure A-17 for a schematic diagram.) The second mixer consists basically of an AGC amplifier, a gain control input OR gate, an AGC linearizer circuit, a double-balanced second mixer, and the IF bandwidth gates.

(1) AGC Amplifier. - The AGC amplifier provides gain between the AGC detector on detector board A13 (see figure 4-3) and the AGC linearizer, and also provides the AGC attack and decay time constants.

(a) If the input at pin 6 is unchanging, diode CR4 is forward-biased and the voltage at the junction of resistor R12 and capacitor C6 will follow or "track" the voltage at the AGC input on pin 6. The complementary-pair feedback amplifier (Q4, Q5) amplifies the voltage that drives the AGC linearizer.

(b) If the voltage at pin 6 increases due to an increase in the rf signal at one of the antenna inputs the voltage at the junction of R12 and C6 will be delayed in following the voltage at pin 6. There will be a corresponding delay at the complementary-pair feedback amplifier output. This delay is related to the AGC attack time and is determined by the values of R12 and C6 and the AGC loop gain.

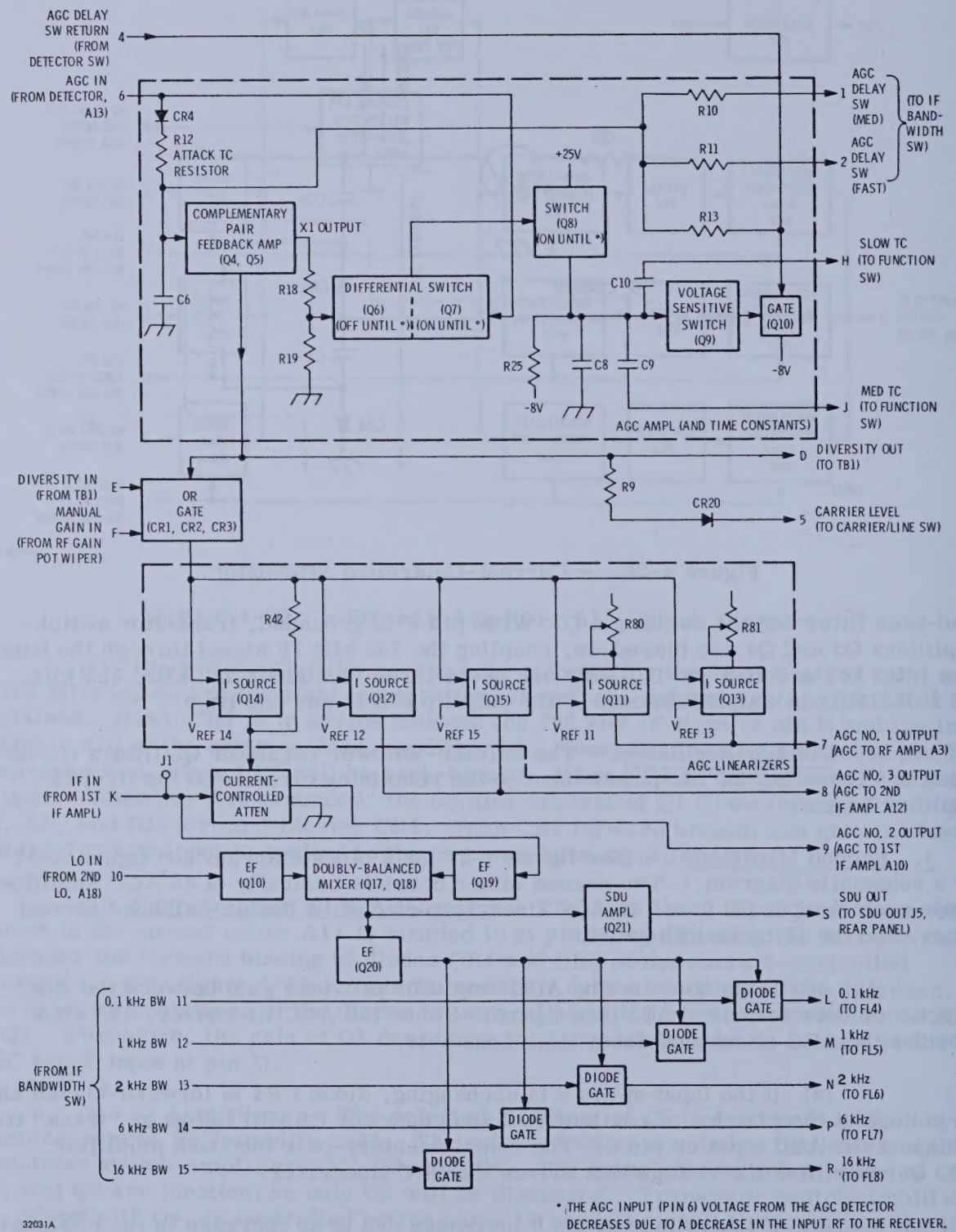


Figure 4-27. – Second Mixer A11, Block Diagram.

(c) To explain the operation of the time delays when the voltage at pin 6 decreases, the circuit is first examined for an unchanging voltage at pin 6. The voltage at the base of Q7 is identical to the voltage at pin 6. The voltage at the base of Q6 will be more negative than the voltage at the base of Q7, due to the diode drop at CR4, the emitter-base junction drop of Q4, and the voltage drop of R18. This will cause Q6 to be on and Q7 to be saturated on. The collector current of Q7 causes Q8 to be saturated on. This causes the capacitor C8 to be charged to nearly +25 V. Transistor Q9 is cut off, since the base of Q9 must be more negative than 11.8 (±2.0) V for Q9 to be turned on. With Q9 off, the gate (Q10) is open.

(d) When the signal at pin 6 decreases, diode CR4 back-biases, trapping the charge on C6. The voltage on C6 will not change as long as the gate in the discharge path is open. The voltage at the base of Q6 also remains unchanged. The voltage at the base of Q6, however, has decreased. If the new voltage at the base of Q7 is less than the voltage at the base of Q6, then Q6 switches on while Q7 switches off. With no collector current in Q7, Q8 switches off. The charge on C8, then discharges through R25, which is connected to -8 V. The voltage on C8, which was originally almost +25 V, is then decreasing toward -8 V. When this voltage is +11.8 (±2.0) V, Q9 turns on. (Q9 base is less than the voltage at the junction of VR2 and R26 minus a diode voltage drop at CR8, and an emitter-base junction voltage drop at Q9.) Collector current from Q9 turns on the Q10 gate and provides a discharge path for CR6 through R13 to the -8 V supply. This time-period from the decrease of the voltage at pin 6, until the Q10 gate closes is the first part of the two-part time delay that makes up the AGC decay time. The first part of the time delay is determined by the values of R28 and C8. The voltage on C6 is decreasing while the discharge is occurring through R28. There is a corresponding voltage change at output of the complementary-pair feedback amplifier (Q4, Q5) which drives the AGC linearizer.

When the voltage on C6 becomes less than the voltage at pin 6, the diode CR4 conducts, and the voltage on C6 stops changing. The output of the complementary-pair feedback amplifier (Q4, Q5) also stops changing. The time delay from the turn-on of Q9 gate until the new final value on Q6 (second part of two-part AGC decay time) is determined by the values of C6, R13, and the AGC loop gain.

(e) The AGC "attack time" is independent of front panel switch positions. The AGC decay time is dependent on the front panel FUNCTION, DETECTOR, and IF BANDWIDTH switch positions. The first part of the two-part AGC decay time is altered by either the grounding of medium time constant at pin J or the grounding of slow time constant at pin H. This action will place either C9 or C10 in parallel with C8. The second part of the two-part AGC decay time is altered by either the shorting of pin 1 to pin 4 or the shorting of pin 2 to pin 4. This action will place either R10 or R11 in parallel with R13. The following tables, 4-5 and 4-6, show the relationship of the FUNCTION, DETECTOR, and IF BANDWIDTH switch positions to the two-part AGC decay time.

Table 4-5. – First Part of AGC Decay Time.

FUNCTION SWITCH	AGC-F	AGC-M, SQUELCH	AGC-S
Capacitor in parallel with C8	none	C9	C10
Relative discharge rate	fast	medium	slow

Table 4-6. – Second Part of AGC Decay Time.

		DETECTOR SWITCH		
		AM/BFO, AM, CW OR FM	LSB OR USB	ISB 3KHZ OR ISB 6 KHZ
BANDWIDTH	0.1	none (slow)	R10 (medium)	R11 (fast)
	1.0	R10 (medium)	R10 (medium)	R11 (fast)
	2,6,16	R11 (fast)	R10 (medium)	R11 (fast)

Note: – Resistance in parallel with R13 and relative discharge rate.

(f) The AGC output of feedback amplifier (Q4, Q5) is also available as the carrier level output at pin 5 and the diversity output at pin D. The carrier level AGC output, which is proportional to the IF signal level, is coupled to the CARRIER-LINE meter M1 via the CARRIER-OFF-LINE switch S5. This carrier level output is available for RF input levels to the receiver above an AGC threshold level. Below an AGC threshold level a carrier level output from detector A13 supplies an output to the CARRIER-LINE mater. The diversity AGC output is available at DIVERSITY OUT terminal TB1-11 on the rear panel. When used as the main tuning receiver, during diversite reception, this AGC voltage is coupled to the slave receiver.

(2) OR gate. - The OR gate consisting of CR1, CR2, and CR3 will pass only the largest (most positive) of the three input voltages (AGC amplifier output, manual input, or diversity input). A larger voltage at the output of the OR gate will cause the RF and IF gain to be decreased by the current-controlled attenuators in the RF amplifier A3, first IF amplifier A10, second mixer A11, and second IF amplifier A12. If the FUNCTION switch is in MGC, the AGC disable (pin 8 of the detector A13) is activated, disabling the AGC detector. Correspondingly, there will be no output from the AGC amplifier. Therefore, the RF gain voltage at pin F will control the receiver gain. When the FUNCTION switch is in AGC F, AGC M, or AGC S, the output of the AGC amplifier will take over control of the receiver gain, when that output voltage exceeds the RF gain voltage input at pin F. Therefore, AGC action can never cause the gain to be greater than the gain as set by the RF GAIN control on the front panel. When the receiver is coupled with another receiver for diversity reception, and this receiver is not used for main tuning, an AGC input is coupled in at pin E from the main tuning receiver via DIVERSITY IN terminal TB1-10 on the rear panel.

(3) AGC Linearizers. - The AGC linearizers convert the voltage from the AGC amplifier to currents to drive the current-controlled attenuators on the RF amplifier A3, first IF amplifier A10, second mixer A11, and second IF amplifier A12. The AGC linearizers also convert the voltage of the AGC amplifier to currents in a piece-wise linear manner. This nonlinear conversion of voltage to current is matched to the nonlinear gain change versus current (db/ma) of the current-controlled (db/V). The bias resistors R32 and R33 of current-source Q12 set a permanently fixed voltage ($V_{Rrf\ 12}$) at the base of Q12. The output of the OR gate (CR1, CR2, CR3) must exceed the emitter-base junction voltage drop of Q12 and the junction voltage drop of CR10 before there will be any current at the collector of current source Q12. The current at the collector of current-source Q12 will then be proportional to ($V_{OR\ gate} - V_{Ref\ 12}$ -2 junction voltage drops). Transistors Q11, Q13, Q14, and

Q15 operate in the same manner. Resistor R42 can also be considered a current source.

(4) FET Double-Balanced Mixer. - The LO voltage is buffered by Q16 and applied to the gate of Q17 and the source of Q18. The LO voltage is large enough to drive the FET's from the on condition to cut-off. The IF voltage is buffered by Q19 and applied to the source of Q17 and the gate of Q18. The two drains are connected together to provide the mixer output which is buffered by transistor stage Q20. SDU amplifier Q21 provides 455 kHz IF output at pin S to the SDU OUT connector J5 on the rear panel.

(5) IF Bandwidth Gates. - The 100 kHz, 1 kHz, 2 kHz, 6 kHz, and 16 kHz IF bandwidth gates are identical in operation, therefore only the 100 Hz IF bandwidth gate will be discussed. When the 100 Hz bandwidth control input at pin 11 is grounded, diode CR15 will be forward-biased by the emitter current of transistor Q20, and the junction of CR15 and R64 will be at 5.7 (±1.5) V. The forward-biased diode CR15 presents a low impedance path from R64 to the 100 Hz bandwidth output at pin L. Resistors R64 and R70 combine to provide a source impedance at the 100 Hz bandwidth output at pin L to match the 500 ohm input impedance of the 100 Hz bandwidth, 455 kHz center frequency filter FL4. When the 100 Hz bandwidth control input at pin 11 is open-circuited, there is no current flow through CR15, and CR15 presents a high series impedance between R64 and the 100 Hz bandwidth output at pin L.

k. Second Local Oscillator A18. - The second level oscillator A18 provides any one of the following three output frequencies to the second mixer A11.

3217 kHz (±15 Hz)
1217 kHz (±20 Hz)
847 kHz (±30 Hz)

One of these three output frequencies is selected for coupling to the second mixer A11 by remote switching (GRD potential) from part of the BAND-MHZ switch on AFC board A8. Refer to table 4-7 for comparisons of the frequency band, IF, and second LO frequencies. Three screwdriver adjustments are provided on the second LO assembly for initial or corrective adjustments of the three LO frequency outputs. A FINE TUNE control is located on the front panel of fine tuning of the input frequency.

Table 4-7. – IF and LO Frequencies.

FREQUENCY BAND (MHz)	FIRST IF FREQUENCIES (MHz)	SECOND LO FREQUENCIES (MHz)	FINAL IF FREQUENCY (kHz)
1.5-2.7	0.392	0.847	455
2.7-5	0.762	1.217	455
5-9	0.762	1.217	455
9-17	2.762	3.217	455
17-32	2.762	3.217	455

l. Second IF Amplifier A12. - (See figure 4-28 for a block diagram and figure A-18 for a schematic diagram.) The second IF amplifier consists basically of IF amplifiers, a diode gate circuit for selecting the required IF bandwidth, a current-controlled attenuator for controlling the gain of the IF amplifiers, and a line meter amplifier and detector circuit.

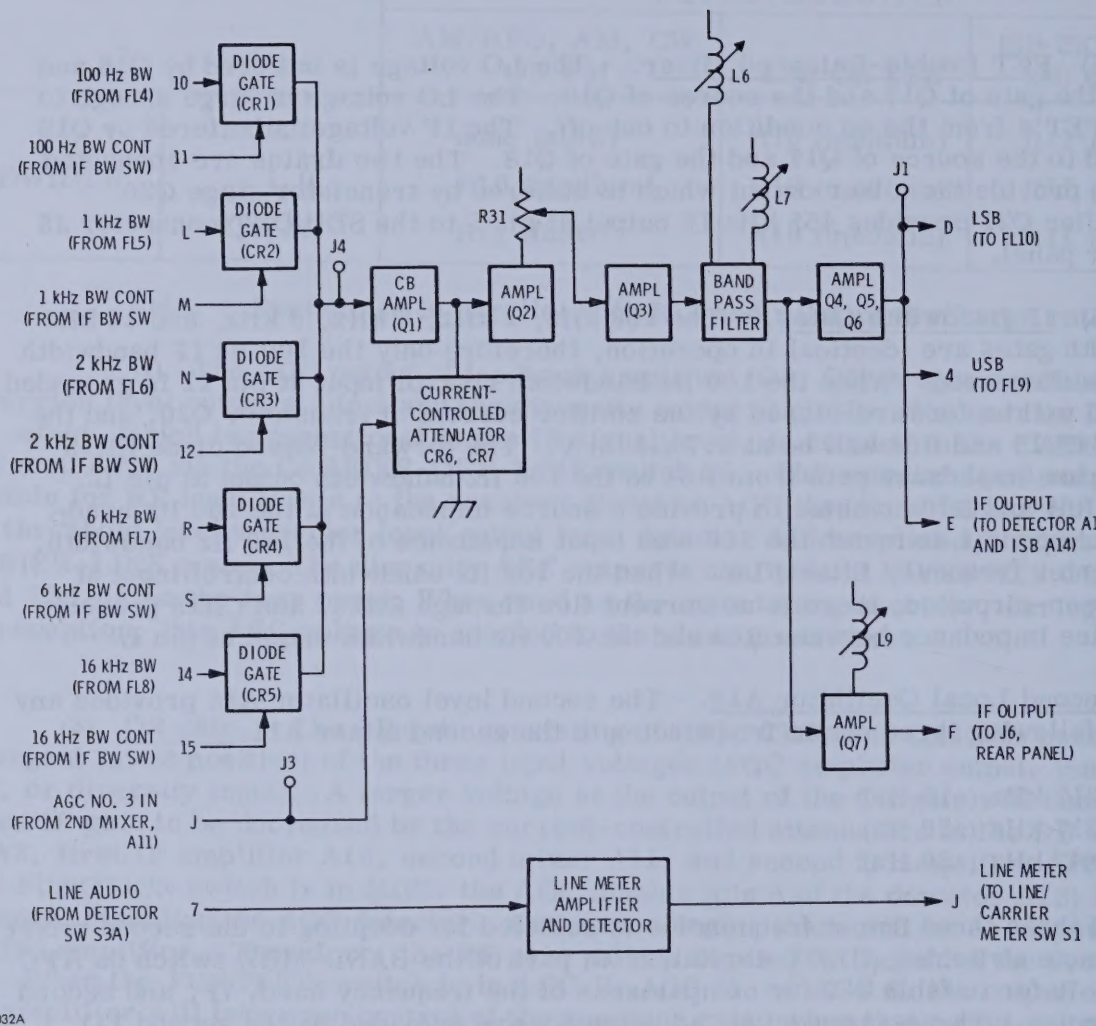


Figure 4-28. – Second IF Amplifier A12, Block Diagram.

(1) Diode Gate Circuits. - The gate circuits for the 100 Hz, 1 kHz, 2 kHz, 6 kHz, and 16 kHz bandwidth inputs are identical in operation, therefore only one gate circuit will be explained. The center frequency for each input is 455 kHz. Diode CR1 is in series between the 100 Hz bandwidth input at pin 10 and the input resistor R22 to the common-base amplifier Q1. When pin 11 is open-circuited, diode CR1 will become back-biased. When diode CR11 is back-biased, the gate is open. When pin 11 is grounded, the emitter current of Q1 flows through R22, CR1, R3, and R2, forward biasing CR1. With CR1 forward-biased, the gate is closed and the 455 kHz IF with bandwidth of 100 Hz is applied to the common-base amplifier Q1. Resistors R1 and R3 also attenuate the IF signal between pin 10 and the Q1 input resistor R22.

(2) Current-Controlled Attenuator. - The IF output of common-base amplifier Q1 is amplified by two common-emitter amplifiers Q2 and Q3 prior to passing through the band-pass filter (L6, C30, C31, L7). Between the amplifier stages Q1

and Q2 is located a current-controlled attenuator. The current-controlled attenuator (CR6, CR7) is part of the AGC circuit. The AGC No. 3 input at pin K is driven by a current source in the second mixer. Increasing the dc current causes diodes CR6 and CR7 to become increasingly more forward-biased, which causes their dynamic resistance to decrease. The dynamic resistance of the diodes is in parallel with the collector resistance R25 of Q1. Therefore, the amplifier gain of Q1 decreases for increasing dc input current at pin K.

(3) \ IF Amplifiers. - The IF output of Q3 is coupled through a band-pass filter to the input of Q4 and Q7. Amplifier Q7 provides an IF output through pin F to the IF OUT connector J6 on the rear panel. Transistors Q4 and Q6 form a complementary-pair feedback circuit. IF and dc feedback enhance gain and bias stability. The IF output of this complementary pair is coupled through emitter-follower Q6 to output pins D, 4, and E. The output at pin D is connected to LSB filter FL10. The IF output at pin E is connected to the inputs of detector A13 and ISB A14.

m. Detector A13. - (See figure 4-29 for a block diagram and figure A-19 for a schematic diagram.) The detector consists basically of IF amplifiers, AGC detector, AM detector, a diode gate circuit, USB product detector, and a cw product detector.

(1) Diode Gates. - Three diode gates control the IF inputs to the AGC amplifier and detector circuit. These are the USB gate (CR1 and CR3), the DSB gate (CR2 and CR4), and the LSB gate (CR4 on ISB A14 and CR5). Only the USB gate will be explained because the other gates are identical. When pin N is open-circuited, the USB gate (CR1 and CR3) is in the "OFF" state. The current that flows through resistor R4 will forward-bias diode CR1. Diode CR3 will be back-biased. Diode CR1 provides a low-impedance path to ground for the USB IF input through capacitor C3, and CR3 provides a high impedance in series with the common-base amplifier Q6. When pin N is grounded, the USB gate is in the "ON" state. The current that flows through R4 will return to ground via pin N. Diode CR1 will be back-biased because of the lower voltage at the junction of R4 and CR1, and CR3 will be forward-biased by the emitter current of Q6, which also returns to ground through pin N. Diode CR1 is therefore a high impedance to ground while CR3 is a low series impedance for the USB IF input signal to amplifier Q6.

(2) AGC Detector Amplifier. - Transistor Q6 is connected as a common-base amplifier with an input impedance set by input resistors from each IF input; such as, the 620 ohm resistor R3 for the USB gate. The IF output of Q6 is coupled to amplifier Q7. Transistor Q7 is a common-emitter amplifier with unbypassed emitter resistance. The unbypassed emitter resistance reduces the gain of Q7 by degenerative feedback. Increasing the unbypassed emitter resistance reduces the gain of Q7. The source-to-gate dynamic resistance of the FET transistor Q8 is the unbypassed emitter resistance of Q7. Since the source-to-gate resistance increases as source current decreases, the amplifier gain can be controlled by adjusting the source current. The source current can be controlled by the value of resistance between the AGC threshold at pin F and -8 V. A resistor may be connected between pin F and -8 V at TB1-12, -13 at the rear panel. A small value of resistance causes high gain in transistor Q7, while a large value of resistance causes low gain in Q7. These AGC threshold resistor values (if required) are selected experimentally. The AGC threshold is accomplished by gain controlling Q7 and Q9 before the AGC detector. The actual threshold circuit (a diode in the second mixer) operates when the output of

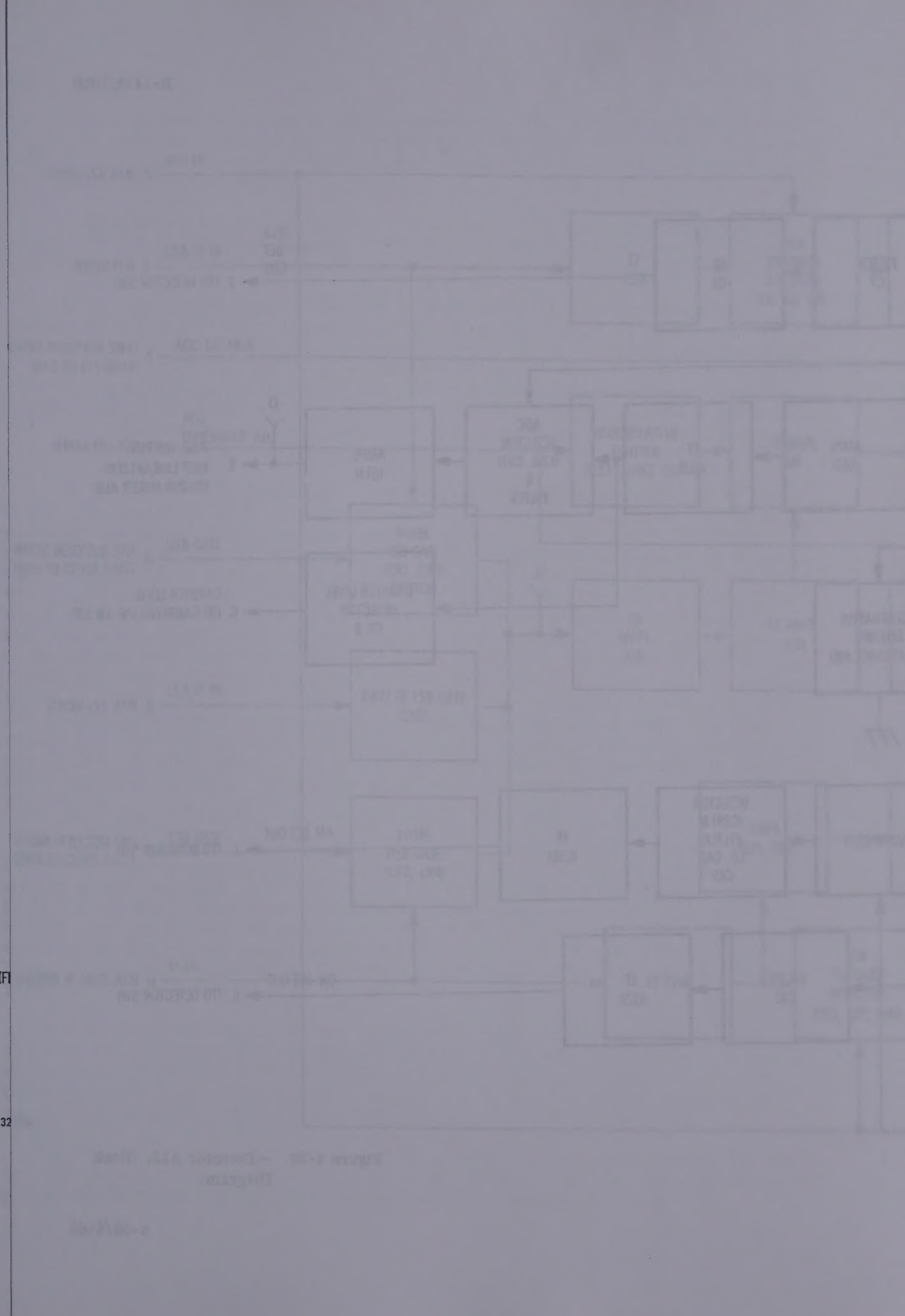
the amplifier Q13 exceeds zero dc. The IF output from Q9 is further amplified by Q11 and coupled through emitter-follower Q12 to the input of AGC detector CR6 and CR7 and to the carrier level detector CR8. The carrier level output is available to the CARRIER-LINE meter when the RF signal input to the receiver is below an AGC threshold level. Above this AGC threshold level a carrier level output from second mixer A11 is available.

(3) AGC Detector. - Diodes CR6 and CR7 form a voltage doubling detector. The voltage developed across resistor R49 by the detector is impressed across resistor R50. But the current flow through R50 also flows through resistor R48. The result is that the detector output voltage is amplified by (R50 + R48)/R50 in the transistor stage. The output at transistor Q13 is therefore -8 V for no IF signal from transistor Q12 and is increasingly more positive as the IF signal from Q12 increases.

(4) IF Amplifier and AM Detector. - The IF input at pin H is also coupled to an AM detection circuit and to a continuous wave (cw) product detector. The IF input at pin H is first coupled through emitter-follower Q14 to IF amplifier Q15 and to transistor Q20. Transistors Q15, Q16, and Q17 are common-emitter IF amplifier stages. Transistor Q17 also amplifies the BFO input when it is injected at the emitter of Q17. Transistor Q17 acts as a linear combiner of the IF signal and the BFO input. The output of Q17 is detected by diode CR9. The detected output from CR9 is filtered and coupled through emitter-follower Q18 to pin J as the AM detector output. The output of Q18 is approximately zero for no IF signal present and is increasingly more positive as the IF signal from Q17 increases.

(5) CW Product Detector. - The IF input from emitter-follower Q14 is also coupled to CW product detector (Q20, Q21, Q22). Transistors Q21 and Q22 form a differential pair with transistor Q20 operating as a current source. The current of Q20 will be proportional to the IF input signal. When the BFO voltage is not present, the IF signal current of Q20 divides between Q21 and Q22. The filter capacitor C7, effectively bypasses collector resistor R90 at IF frequencies, so there will be no output voltage at the emitter of Q23. When the BFO voltage is present from pins, the IF signal current is switched between Q3 and Q4 at the frequency of the BFO. The current through Q22 is, therefore, IF signal current that is chopped at the BFO frequency. Switching Q20 from the on to off state is a nonlinear operation that causes mixing between the IF signal and the BFO signal. The AM modulation on the IF signal is down-converted to audio frequencies. The filter capacitor C53 is high impedance to the audio frequency and the voltage is developed across R90. Emitter-follower Q23 couples the CW product detector output to pin K, which is connected to the front panel DETECTOR switch.

(6) USB Product Detector. - The USB IF input at pin L is also coupled to emitter-follower Q1 and then to the USB product detector (Q2, Q3, Q4). Transistors Q3 and Q4 form a differential pair with transistor Q2 operating as a current source. The current of Q2 will be proportional to the USB IF input signal. When the BFO voltage is not present, the IF signal current of Q2 divides between Q3 and Q4. The filter capacitor C7, effectively bypasses collector resistor R13 at IF frequencies, so there will be no output voltage at the emitter of Q5. When the BFO voltage is present from pin S, the IF signal current is switched between Q3 and Q4 at the frequency of the BFO. The current through Q4 is, therefore, IF signal current that is chopped at the BFO frequency. Switching Q2 from the on to the off state is a nonlinear operation that causes mixing between the IF signal and the BFO signal. The AM modulation on



the amplifier Q13 exceeds zero dc. The IF output from Q9 is further amplified by Q11 and coupled through emitter-follower Q12 to the input of AGC detector CR6 and CR7 and to the carrier level detector CR8. The carrier level output is available to the CARRIER-LINE meter when the RF signal input to the receiver is below an AGC threshold level. Above this AGC threshold level a carrier level output from second mixer A11 is available.

(3) AGC Detector. - Diodes CR6 and CR7 form a voltage doubling detector. The voltage developed across resistor R49 by the detector is impressed across resistor R50. But the current flow through R50 also flows through resistor R48. The result is that the detector output voltage is amplified by (R50 + R48)/R50 in the transistor stage. The output at transistor Q13 is therefore -8 V for no IF signal from transistor Q12 and is increasingly more positive as the IF signal from Q12 increases.

(4) IF Amplifier and AM Detector. - The IF input at pin H is also coupled to an AM detection circuit and to a continuous wave (cw) product detector. The IF input at pin H is first coupled through emitter-follower Q14 to IF amplifier Q15 and to transistor Q20. Transistors Q15, Q16, and Q17 are common-emitter IF amplifier stages. Transistor Q17 also amplifies the BFO input when it is injected at the emitter of Q17. Transistor Q17 acts as a linear combiner of the IF signal and the BFO input. The output of Q17 is detected by diode CR9. The detected output from CR9 is filtered and coupled through emitter-follower Q18 to pin J as the AM detector output. The output of Q18 is approximately zero for no IF signal present and is increasingly more positive as the IF signal from Q17 increases.

(5) CW Product Detector. - The IF input from emitter-follower Q14 is also coupled to CW product detector (Q20, Q21, Q22). Transistors Q21 and Q22 form a differential pair with transistor Q20 operating as a current source. The current of Q20 will be proportional to the IF input signal. When the BFO voltage is not present, the IF signal current of Q20 divides between Q21 and Q22. The filter capacitor C7, effectively bypasses collector resistor R90 at IF frequencies, so there will be no output voltage at the emitter of Q23. When the BFO voltage is present from pins, the IF signal current is switched between Q3 and Q4 at the frequency of the BFO. The current through Q22 is, therefore, IF signal current that is chopped at the BFO frequency. Switching Q20 from the on to off state is a nonlinear operation that causes mixing between the IF signal and the BFO signal. The AM modulation on the IF signal is down-converted to audio frequencies. The filter capacitor C53 is high impedance to the audio frequency and the voltage is developed across R90. Emitter-follower Q23 couples the CW product detector output to pin K, which is connected to the front panel DETECTOR switch.

(6) USB Product Detector. - The USB IF input at pin L is also coupled to emitter-follower Q1 and then to the USB product detector (Q2, Q3, Q4). Transistors Q3 and Q4 form a differential pair with transistor Q2 operating as a current source. The current of Q2 will be proportional to the USB IF input signal. When the BFO voltage is not present, the IF signal current of Q2 divides between Q3 and Q4. The filter capacitor C7, effectively bypasses collector resistor R13 at IF frequencies, so there will be no output voltage at the emitter of Q5. When the BFO voltage is present from pin S, the IF signal current is switched between Q3 and Q4 at the frequency of the BFO. The current through Q4 is, therefore, IF signal current that is chopped at the BFO frequency. Switching Q2 from the on to the off state is a nonlinear operation that causes mixing between the IF signal and the BFO signal. The AM modulation on

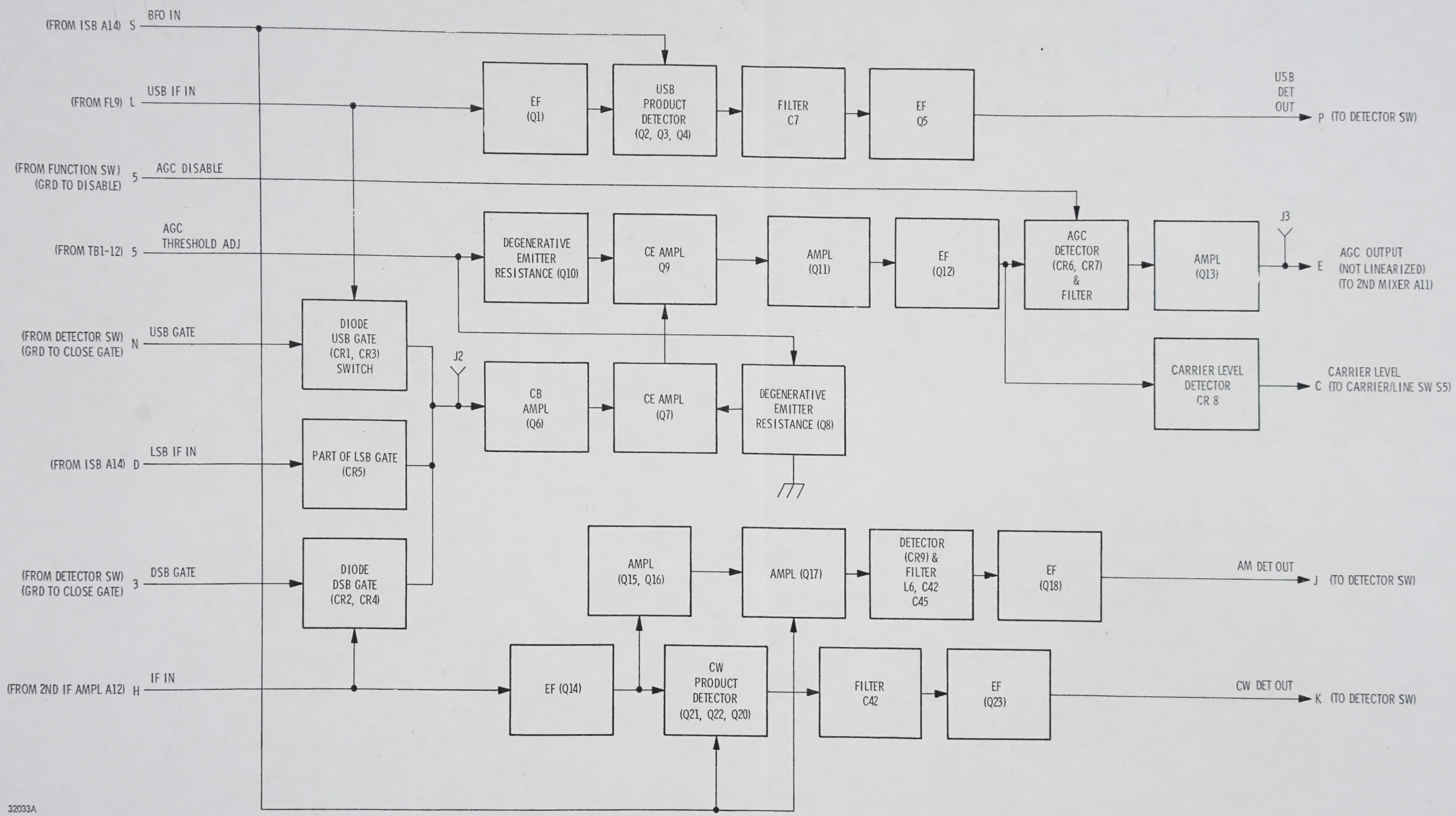


Figure 4-29. – Detector A13, Block Diagram.

the IF signal is down-converted to audio frequencies. The filter capacitor C7 is high impedance to the audio frequency and the voltage is developed across R13. Emitter-follower Q5 couples the USB product detector output to pin P which is connected to the front panel DETECTOR switch.

n. Independent Sideband (ISB) A14. - (See figure 4-30 for a block diagram and figure A-20 for a schematic diagram.) The ISB consists basically of an LSB product detector, audio amplifiers for the LSB audio, IF amplifiers, and an FM detector.

(1) LSB Diode Gate. - The LSB IF input at pin M is coupled to emitter-follower Q1 and to a diode gate consisting of CR1 on A14 and CR5 on detector A13. When pin 9 is open-circuited, CR1 is forward-biased and diode CR5 on detector A13 is back-biased. The LSB gate is now in the "OFF" state with CR1 providing a low-impedance path through C9 to ground and CR5 on detector A13 providing a high impedance in series with first AGC IF amplifier on detector A13. When pin 9 is grounded, CR1 is back-biased and CR5 on detector A13 is forward-biased. The LSB IF is now coupled directly through pin 8 to the input of the AGC IF amplifier on detector A13.

(2) LSB Product Detector. - Emitter-follower Q1 couples the LSB IF input to the LSB product detector (Q2, Q3, Q4). Transistors Q3 and Q4 form a differential pair with transistor Q2 operating as a current source. The current at Q2 will be proportional to the LSB IF input signal. When the crystal BFO voltage is not present, the IF signal current of Q2 divides between Q3 and Q4. The filter capacitor C16 effectively bypasses collector resistor R16 at the IF frequencies, therefore there will be no output voltage at the emitter of Q6. When the crystal BFO voltage is present at the base of Q3, the IF signal current is switched between Q3 and Q4 at the frequency of the crystal BFO. The current through Q4 is, therefore, the IF signal current that is chopped at the BFO frequency. Switching Q2 from the on to the off state is a non-linear operation that causes mixing between the IF signal and the crystal BFO. The AM modulation on the IF signal is down converted to audio frequencies. The filter capacitor C10 is high impedance to the audio frequency and the voltage is developed across R16. Emitter-follower Q5 couples the LSB product detector output to pin 10 and to the low-pass filter. The output at pin 10 is connected to the front panel DETECTOR switch.

(3) IF Amplifier and FM Detector. - The IF input at pin 7 is coupled to the common-emitter amplifier Q13. The output of Q13 drives a high gain differential amplifier (Q14 and Q15). The collector of Q17 is fed back through a low-pass filter to the base of Q15. This forms an operational amplifier type circuit (Q14, Q15, Q16, and Q17) for low frequencies only. The effect of the feedback is to provide the bias stability for Q16. There are no feedback effects, however, at the IF frequency. The IF signal at the collector of Q18 drives a parallel resonant tank (L4 and C35), followed by detector CR12 and emitter-follower Q18.

A differential pair is an efficient limiter when operated in a saturated mode. When the input IF signal is large enough to drive the differential amplifier into saturation, the total current is switched from one of the differential pair transistors to the other at the frequency of the input signal. Therefore, the output voltage of one collector of the differential amplifier is independent of input voltage level.

The frequency sensitive character of the parallel resonant circuit forms the FM detector characteristic as shown in figure 4-31. Diodes CR10 and CR11 are primarily protection diodes for Q16 and Q17, but they also provide some limiting.

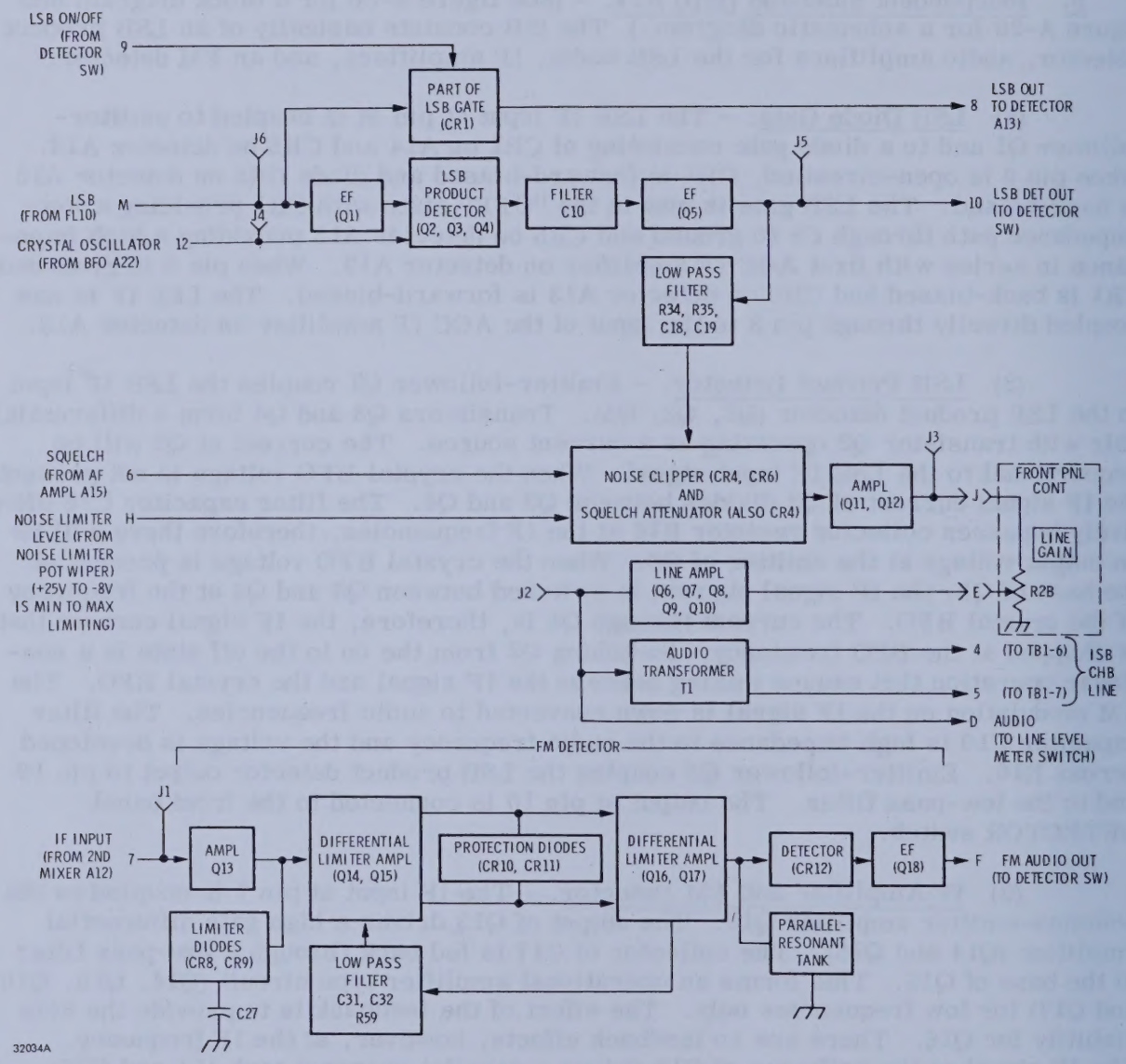


Figure 4-30. – Independent Sideband (ISB) A14, Block Diagram.

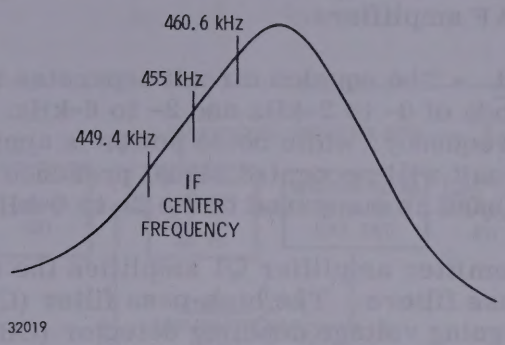


Figure 4-31. – FM Detector Characteristic

(4) Squelch Attenuator. - When the FUNCTION switch on the front panel is not in the SQUELCH position, a high positive voltage input at pin 6 back-biases diode CR7. Diode CR4 is also back-biased resulting in no attenuation of the signal from the low-pass filter. When the FUNCTION switch is in the SQUELCH position and no audio signal is present, the high positive voltage at pin 6 is replaced with approximately -7 volts from the squelch circuit on AF amplifier A15. This causes both CR4 and CR7 to become forward-biased. Diode CR4 will then cause attenuation of the noise in the main signal path that is applied to the base of transistor Q11, by providing a low impedance path to ground. The input to Q11 is available from the LSB product detector via the low-pass filter. When the threshold of the squelch circuit on AF amplifier A15 is exceeded, the output of the squelch circuit is switched to approximately ±14 volts. This back-biases CR7 and removes the low impedance path to ground through CR4.

(5) AF Amplifiers. - The feedback-pair amplifier consisting of Q11 and Q12 preamplifies the input LSB audio signal from the low-pass filter. The output of this preamplifier stage is coupled out at pin J through part of the LINE GAIN potentiometer R2, located on the front panel, and back through pin E of ISB 14 to the line audio amplifier (Q6, Q7, Q8, Q9, Q10). The transistor stage of Q6 is a high gain, common-emitter amplifier which drives the transistor pair (Q9 and Q10) and the complementary pair (Q7 and Q8). These two transistor pairs provide high current, push-pull operation. The feedback resistor R22, which is connected between the amplifier output and the base of Q6, reduces the gain but provides gain stability and greater linear dynamic range. The output of the line audio amplifier drives the audio transformer T1. The audio transformer secondary is connected to the LINE OUT CH B (ISB) at TB1-6, -7 on the rear panel.

(6) Noise Limiting. - The noise limiting action is produced by the biasing of CR4 and CR6. When the NOISE LIMITER control on the front panel is adjusted so that +25 volts is connected to pin H, diodes CR4 and CR6 are back-biased. There will be no clipping of the signal available at the base of Q11, because of the noise limiting diodes during this condition. Reduction of the positive voltage at pin H, by adjusting the NOISE LIMITER control will allow the peaks of the signal at the base to exceed the back-bias voltage at diodes CR4 and CR6. The positive voltage peaks will be clipped by CR6 and the negative peaks will be clipped by CR7.

o. AF Amplifier A15. - (See figure 4-32 for a block diagram and figure A-21 for a schematic diagram.) The AF amplifier consists basically of a squelch circuit, noise limiting circuit, and AF amplifiers.

(1) Squelch Circuit. - The squelch circuit separates the incoming audio power into the frequency bands of 0- to 2-kHz and 2- to 6-kHz. The audio signals are primarily below the 2 kHz frequency, while noise power is approximately equal in the two bands. The squelch circuit will recognize signal presence because of an increase in power of the 0- to 2-kHz band as compared to the 2- to 6-kHz band.

(a) Common-emitter amplifier Q1 amplifies the audio input at pin 7 and drives high-pass and low-pass filters. The high-pass filter (C3, R6, C5, R8, and C7) is terminated in a negative-going voltage doubling detector (CR3 and CR1). The low-pass filter (R5, C4, R7, C6, and C8) is terminated in a positive-going detector (CR2 and CR4). The output of each detector is added to the reference voltage (V_{REF}) available from squelch sensitivity control R14. The voltage at adder resistor R11 is V_{REF} minus the detected voltage from high-pass filter (V_{HFD}). The voltage at adder resistor R12 is V_{REF} plus V_{LFD}. Therefore, the voltage applied to the input pin 3 of operational amplifier AR1 is $V_{REF} + V_{LFD}/2 + V_{HFD}/2$.

(b) The operational amplifier AR1 will switch output polarities when the input voltage at pin 3 exceeds the threshold voltage at pin 2. When V_{HFD} and V_{LFD} are caused by noise only, the voltage at pin 3 of the operational amplifier AR1 will equal V_{REF}. When a large audio signal is present, $V_{LFD}/2$ will increase causing the total voltage at pin 3 of operational amplifier AR1 to exceed the reference voltage V_{REF}. The signal-to-noise ratio at which the operational amplifier will switch is controlled by the adjustment of squelch sensitivity control R14.

(c) The output of the operational amplifier AR1 will be -7 volts when no audio signal is present. When the FUNCTION switch is not in the SQUELCH position, +25 volts is present at pin 15. The +25 volts overrides the effect of the output voltage at the operational amplifier AR1 and back biases diode CR10. When the function switch is in the squelch position, removing +25 volts from pin 15, and no audio signal is present, the -7 volts at the output (pin b) of AR1 causes diodes CR10 and CR7 to become forward biased. Diode CR7 will then cause attenuation of the noise in the main signal path that is applied to the base of transistor Q2, by providing a low impedance path to ground. The input to the base of Q2 is available from pin 7 via the low-pass filter consisting of R24, C18, R25, and C19. When the threshold of AR1 is exceeded by an audio signal at pin 3, the output of AR1 is switched to +14 volts. This back biases CR10 and removes the low impedance path to ground through CR7. The output of AR1 is also connected to a similar circuit in ISB circuit board A14.

(d) The timing of the squelch circuit is controlled by the capacitor C11 and the condition of the switching diode CR5. When the output of AR1 is negative, CR5 is back-biased virtually disconnecting capacitor C11 from the input of AR1. When the output of AR1 becomes positive, because of the presence of an audio signal, CR5 is forward biased. Capacitor C11 is then effectively connected from the input of AR1 to ground. This causes a time delay for operational amplifier AR1 input voltage with a decreasing signal level. Therefore, the squelch circuit will respond rapidly to an increasing signal level and slower to a decreasing signal level.

(2) Noise Limiting. - The noise limiting action is produced by the biasing of CR7 and CR9. When the NOISE LIMITER control is adjusted so that +25 volts is

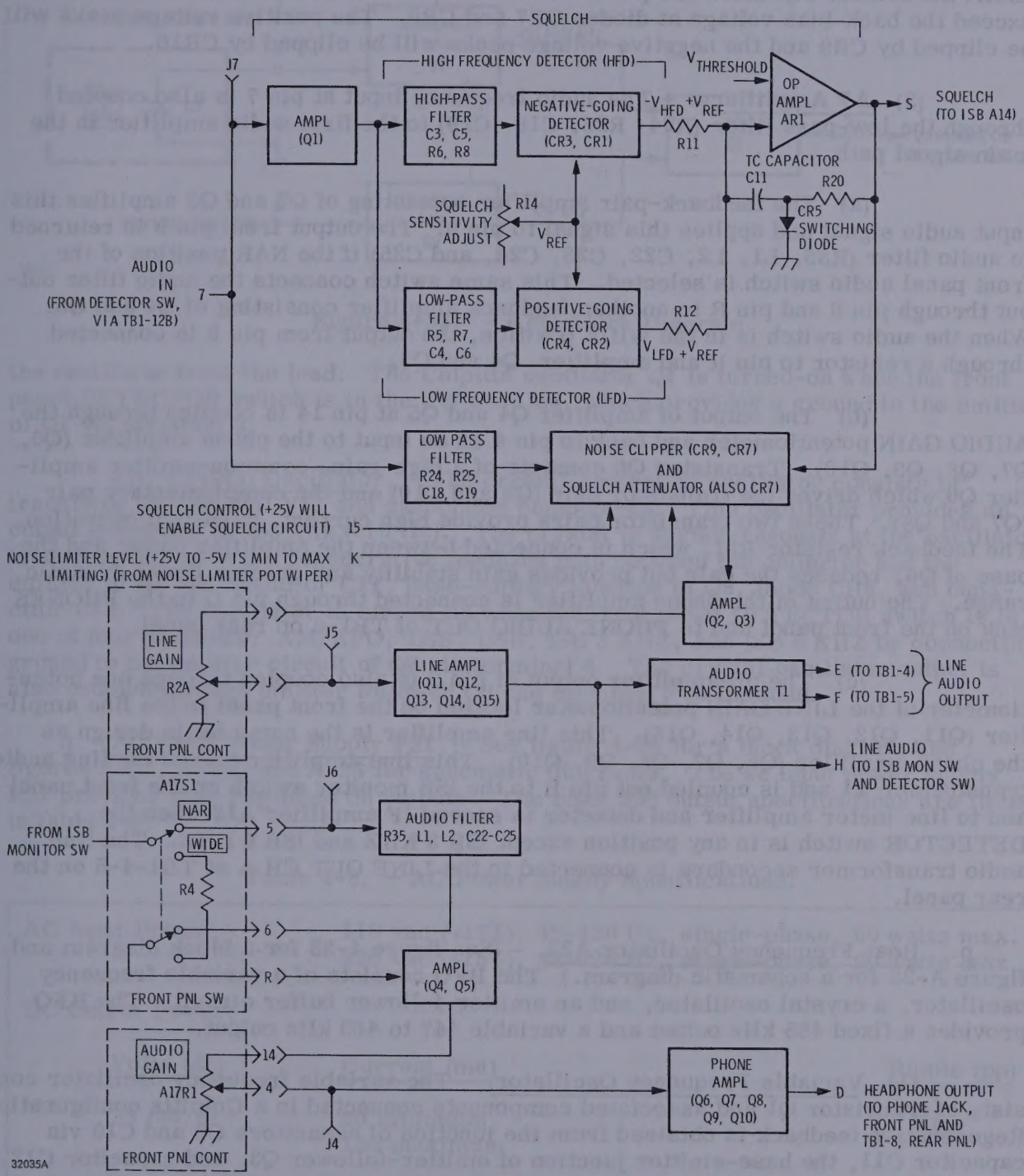


Figure 4-32. – AF Amplifier A15, Block Diagram.

connected to pin K, diodes CR7 and CR9 are back-biased. There will be no clipping of the signal available at the base of Q2 because of the noise limiting diodes during this condition. Reduction of the positive voltage at pin K by adjusting the NOISE LIMITER control will allow the peaks of the waveform available at the base of Q2 to exceed the back-bias voltage at diodes CR7 and CR9. The positive voltage peaks will be clipped by CR9 and the negative voltage peaks will be clipped by CR10.

(3) AF Amplifiers. - The audio frequency input at pin 7 is also coupled through the low-pass filter (R24, R25, C18, C19) to the first audio amplifier in the main signal path.

(a) The feedback-pair amplifier consisting of Q2 and Q3 amplifies this input audio signal and applies this signal to pin 9. The output from pin 9 is returned to audio filter (R35, L1, L2, C22, C23, C24, and C25) if the NAR position of the front panel audio switch is selected. This same switch connects the audio filter output through pin 6 and pin R to another feedback amplifier consisting of Q4 and Q5. When the audio switch is in the WIDE position, the output from pin 9 is connected through a resistor to pin R and amplifier Q4 and Q5.

(b) The output of amplifier Q4 and Q5 at pin 14 is coupled through the AUDIO GAIN potentiometer and back to pin 4 as an input to the phone amplifier (Q6, Q7, Q8, Q9, Q10). Transistor Q6 consists of a high-gain, common-emitter amplifier Q6 which drives the transistor pair (Q9 and Q10) and the complementary pair (Q7 and Q8). These two transistor pairs provide high current, push-pull operation. The feedback resistor R51, which is connected between the amplifier output and the base of Q6, reduces the gain but provides gain stability and greater linear dynamic range. The output of the phone amplifier is connected through pin D to the PHONES jack on the front panel and to PHONE AUDIO OUT of TB1-8 on rear panel.

(c) The preamplifier output at pin 9 is also coupled through one potentiometer of the LINE GAIN potentiometer located on the front panel to the line amplifier (Q11, Q12, Q13, Q14, Q15). This line amplifier is the same basic design as the phone amplifier (Q6, Q7, Q8, Q9, Q10). This line amplifier drives the line audio transformer T1 and is coupled out pin H to the ISB monitor switch on the front panel and to line meter amplifier and detector in second IF amplifier A12 when the DETECTOR switch is in any position except ISB 3 KHZ and ISB 6 KHZ. The line audio transformer secondary is connected to the LINE OUT CH A at TB1-4-5 on the rear panel.

p. Beat Frequency Oscillator A22. - (See figure 4-33 for a block diagram and figure A-22 for a schematic diagram.) The BFO consists of a variable frequency oscillator, a crystal oscillator, and an emitter-follower buffer circuit. The BFO provides a fixed 455 kHz output and a variable 447 to 463 kHz output.

(1) Variable Frequency Oscillator. - The variable frequency oscillator consists of transistor Q1 and associated components connected in a Colpitts configuration. Regenerative feedback is obtained from the junction of capacitors C9 and C10 via capacitor C11, the base-emitter junction of emitter-follower Q3, and capacitor C12. Coil L4 and front panel (BFO kHz) controlled capacitor C2 control the oscillator frequency. Coil L4, located on the board, is the calibration adjustment, and the extend capacitor C2 connected to terminal 6 controls the BFO frequency during operation. The oscillator output is coupled out through terminals from the emitter-follower Q3 emitter resistors R16 and R17. This divided output provides isolation of

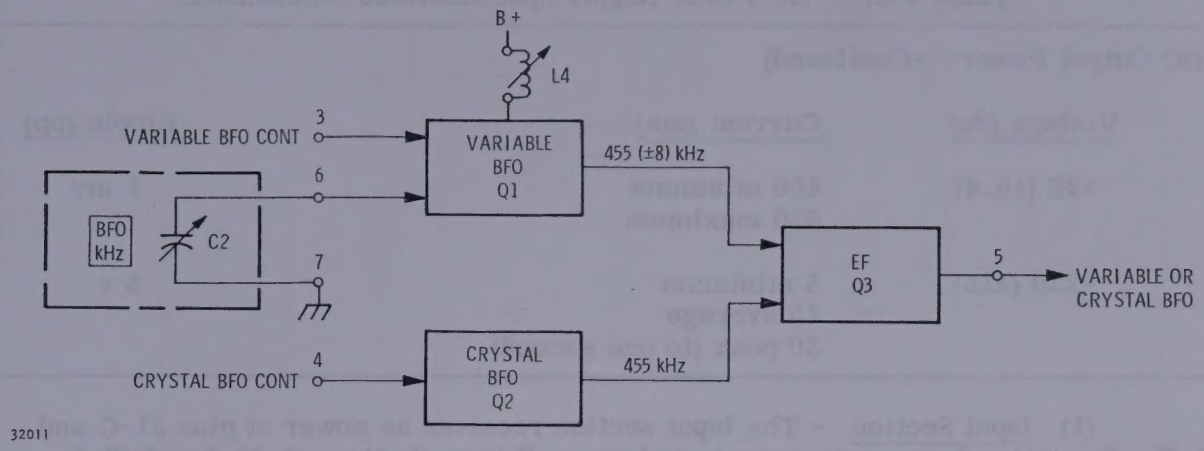


Figure 4-33. – BFO Block Diagram.

the oscillator from the load. The Colpitts oscillator Q1 is turned-on when the front panel DETECTOR switch is in the CW position, which provides a ground to the emitter of Q1 via terminal 3.

(2) Crystal Oscillator. - The crystal-controlled oscillator consists of transistor Q2, crystal Y1, and associated components. This oscillator provides an output frequency of 455 kHz (±10 Hz). The crystal is series-resonant at the oscillator frequency and is in the regenerative feedback path between the collector and the emitter of Q2 via capacitor C11, base-emitter junction of Q3, diode CR6, and capacitor C13. The oscillator is turned-on when the front panel DETECTOR switch is in one of four positions: AM/BFO, LSB, USB, ISB 3 KHZ, and ISB 6 KHZ by connecting ground to the emitter circuit of Q2 via terminal 4. The crystal oscillator output is also coupled through emitter follower Q3 and terminal 5 to the load.

q. AC Input Power Supply PS1. - See figure 4-34 for a block diagram and figures A-23, A-24, and A-25 for schematic diagrams. The ac input power supply PS1 provides four regulated dc outputs. The input and output specifications are listed in table 4-8.

Table 4-8. – AC Power Supply Specifications.

AC Input Power:	110 vac (±15%), 48-420 Hz, single-phase, 60 watts max. 220 vac (±15%), 48-420 Hz, single-phase, 60 watts max.	
DC Output Power:		
Volts (dc)	Current (ma)	Ripple (pp)
-8 (±0.2)	50 minimum 150 maximum	1 mv
+5 (±0.2)	400 minimum 650 maximum	50 mv

Table 4-8. – AC Power Supply Specifications -Continued.

DC Output Power: -Continued)

Voltage (dc)	Current (ma)	Ripple (pp)
+25 (±0.4)	400 minimum 650 maximum	1 mv
+230 (±15)	5 minimum 15 average 30 peak (to one second)	5 v

(1) Input Section. - The input section receives ac power at pins J1-C and J1-F. Provision for remote turn-on and turn-off is made through J2-1 and J2-5. When the receiver FUNCTION switch is in all positions except OFF, these two pins are jumpered. This couples ac power through 1 ampere slow-blow fuses F1 and F2 and through pins J1-E and J1-G to transformer T1. For 220 vac input power, pins J1-D and J1-H are connected together. This connects the input windings of transformer in series. For 110 vac input power, J1-G is connected to J1-D and J1-H is connected to J1-E. This connects to input windings in parallel. The ac input voltages to transformer T1 induce voltages in the multiple secondaries which generate the unregulated dc voltages for the individual regulator sections.

(2) +25 VDC Regulator. - The ac input for the 25 vdc regulator from the transformer secondary via terminals E2 and E3 is rectified by center tap rectifier CR2 and CR4 and is filtered by capacitors C4, C5, C6, C7, C8, and C9. Capacitors C1 and C2 eliminate the communication noise of the rectifiers. The output from the transformer secondary T1 is also rectified by full-wave bridge rectifier CR1, CR2, CR3, and CR4 and is filtered by capacitor C3 to generate a boost (B+) voltage which is reduced and regulated by series dropping resistor R1 and Zener diode VR1. [7,9]

(a) An internal reference voltage is provided by series dropping resistor R6 and Zener diode VR2.[6,9] The output voltage is monitored at voltage divider R12 and R14, which is trimmed by connecting resistors R15 and R16 (points E33 and E34) to points E36 and/or E37 as required. Capacitor C11 provides ac feedback to reduce ripple.

(b) The +25 vdc output voltage is compared with the reference voltage by the action of differential amplifier Q5, Q6. As the output voltage tends to increase, transistor Q6 conducts more, thereby lowering the drive to emitter-follower Q4 and, therefore, to the pass transistor configuration Q1 and Q2. This reduces the output voltage. As the output voltage tends to increase the drive for pass transistors Q1 and Q2 increases, which increases the output voltage. Output capacitor C12 provides a low output impedance at high frequencies and RC network C10 and R11 provides inverse feedback to stabilize the regulator loop and prevent oscillations.

(c) Resistor R4 generates a voltage proportional to the load current, which also appears at the base of transistor Q2. This voltage is applied through resistive divider R2 and R5 to the base of transistor Q3, which is normally biased on the verge of conduction when the power supply is at full load. As the load current increases, the voltage on the base of transistor Q2 rises, which turns on transistor

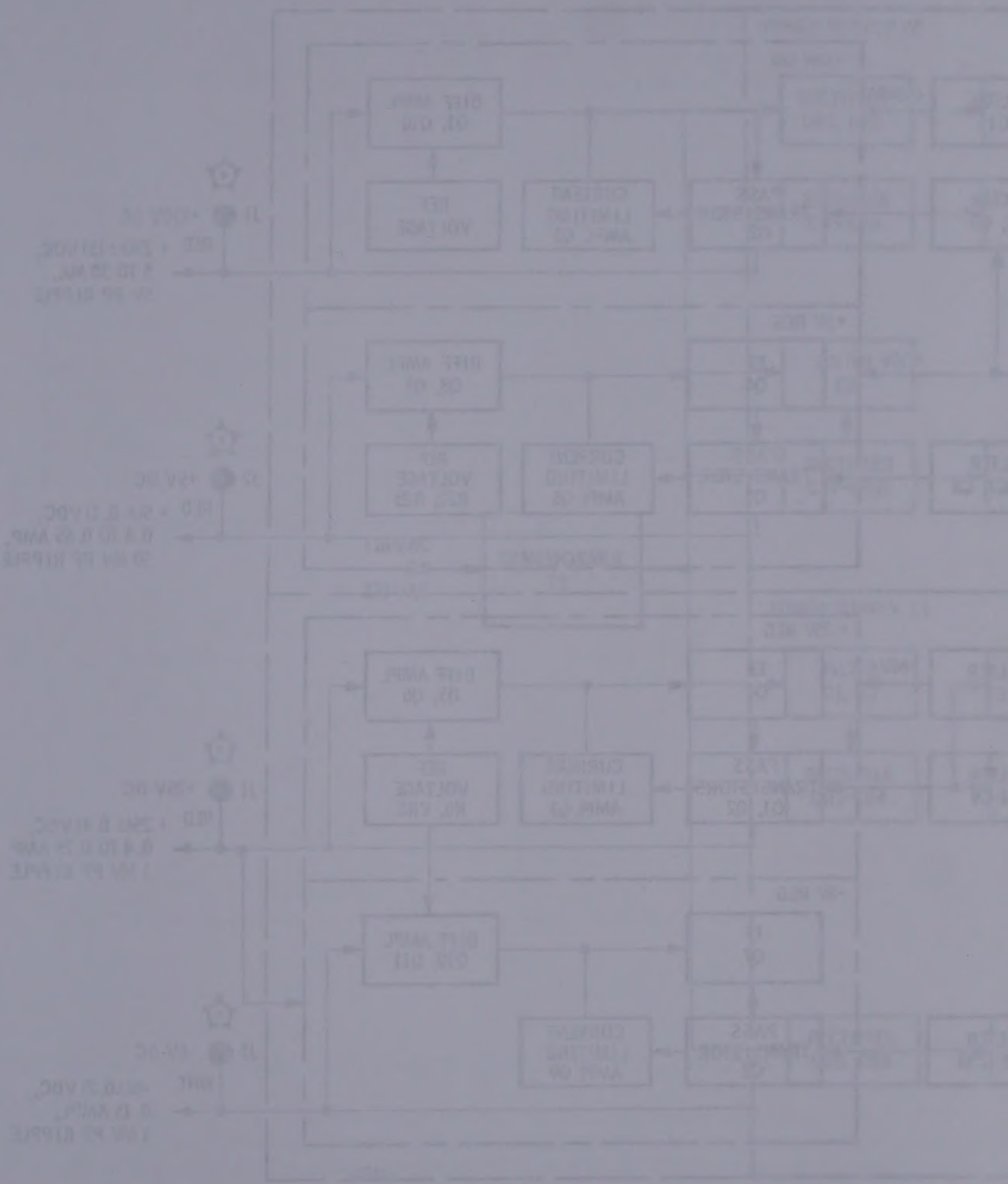


Table 4-8. – AC Power Supply Specifications -Continued.

DC Output Power: -Continued)

Voltage (dc)	Current (ma)	Ripple (pp)
+25 (±0.4)	400 minimum 650 maximum	1 mv
+230 (±15)	5 minimum 15 average 30 peak (to one second)	5 v

(1) Input Section. - The input section receives ac power at pins J1-C and J1-F. Provision for remote turn-on and turn-off is made through J2-1 and J2-5. When the receiver FUNCTION switch is in all positions except OFF, these two pins are jumpered. This couples ac power through 1 ampere slow-blow fuses F1 and F2 and through pins J1-E and J1-G to transformer T1. For 220 vac input power, pins J1-D and J1-H are connected together. This connects the input windings of transformer in series. For 110 vac input power, J1-G is connected to J1-D and J1-H is connected to J1-E. This connects to input windings in parallel. The ac input voltages to transformer T1 induce voltages in the multiple secondaries which generate the unregulated dc voltages for the individual regulator sections.

(2) +25 VDC Regulator. - The ac input for the 25 vdc regulator from the transformer secondary via terminals E2 and E3 is rectified by center tap rectifier CR2 and CR4 and is filtered by capacitors C4, C5, C6, C7, C8, and C9. Capacitors C1 and C2 eliminate the communication noise of the rectifiers. The output from the transformer secondary T1 is also rectified by full-wave bridge rectifier CR1, CR2, CR3, and CR4 and is filtered by capacitor C3 to generate a boost (B+) voltage which is reduced and regulated by series dropping resistor R1 and Zener diode VR1. [7,9]

(a) An internal reference voltage is provided by series dropping resistor R6 and Zener diode VR2.[6,8] The output voltage is monitored at voltage divider R12 and R14, which is trimmed by connecting resistors R15 and R16 (points E33 and E34) to points E36 and/or E37 as required. Capacitor C11 provides ac feedback to reduce ripple.

(b) The +25 vdc output voltage is compared with the reference voltage by the action of differential amplifier Q5, Q6. As the output voltage tends to increase, transistor Q6 conducts more, thereby lowering the drive to emitter-follower Q4 and, therefore, to the pass transistor configuration Q1 and Q2. This reduces the output voltage. As the output voltage tends to increase the drive for pass transistors Q1 and Q2 increases, which increases the output voltage. Output capacitor C12 provides a low output impedance at high frequencies and RC network C10 and R11 provides inverse feedback to stabilize the regulator loop and prevent oscillations.

(c) Resistor R4 generates a voltage proportional to the load current, which also appears at the base of transistor Q2. This voltage is applied through resistive divider R2 and R5 to the base of transistor Q3, which is normally biased on the verge of conduction when the power supply is at full load. As the load current increases, the voltage on the base of transistor Q2 rises, which turns on transistor

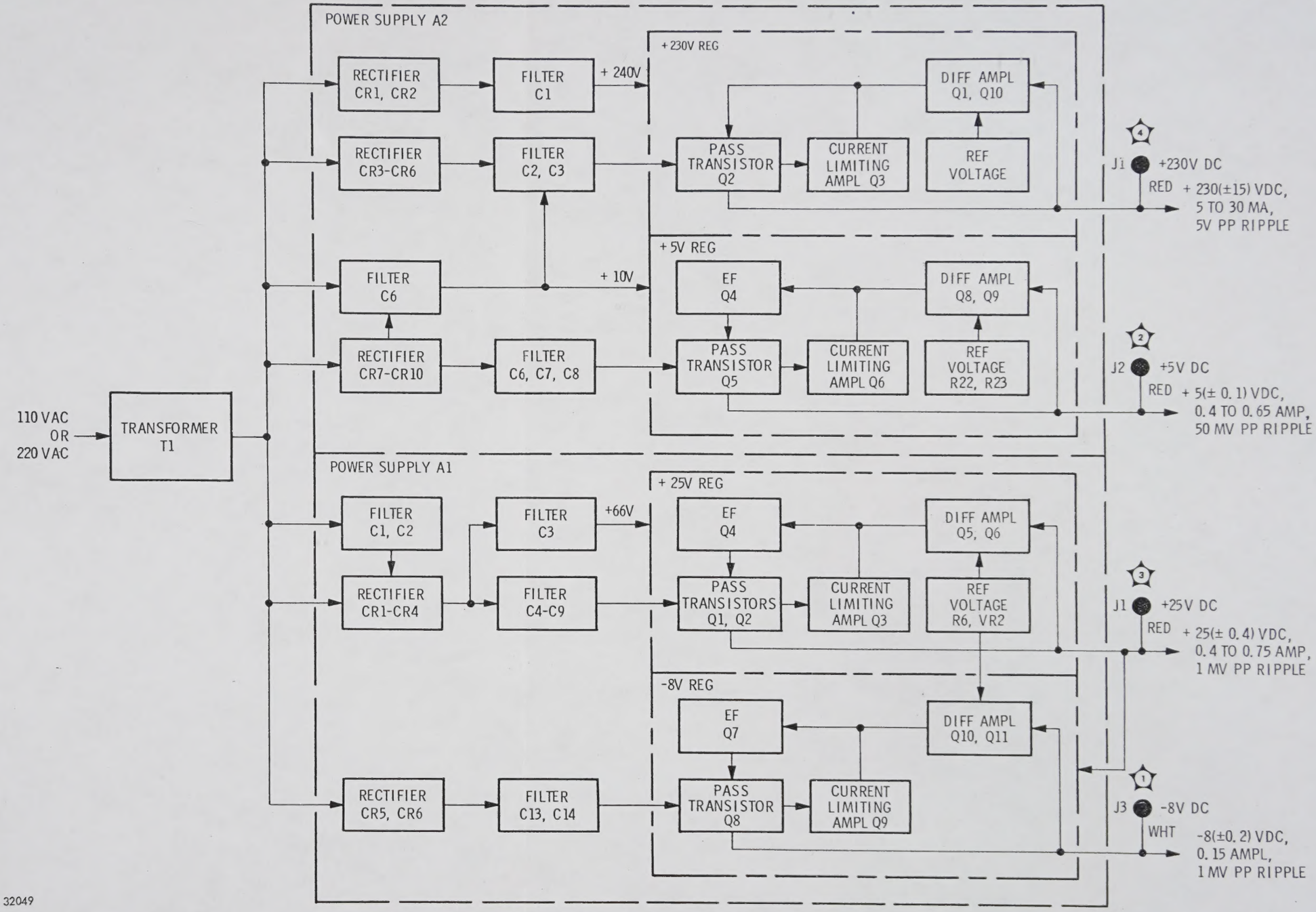


Figure 4-34. – Power Supply PS1, Block Diagram.

Q3, thereby lowering the drive to transistor Q4 and the pass transistor configuration, and the power supply enters a current limiting mode of operation. If further load is applied, the output voltage falls, and the action of the voltage divider network R2 and R5 generates the current limit bendback characteristics shown in figure 4-35.

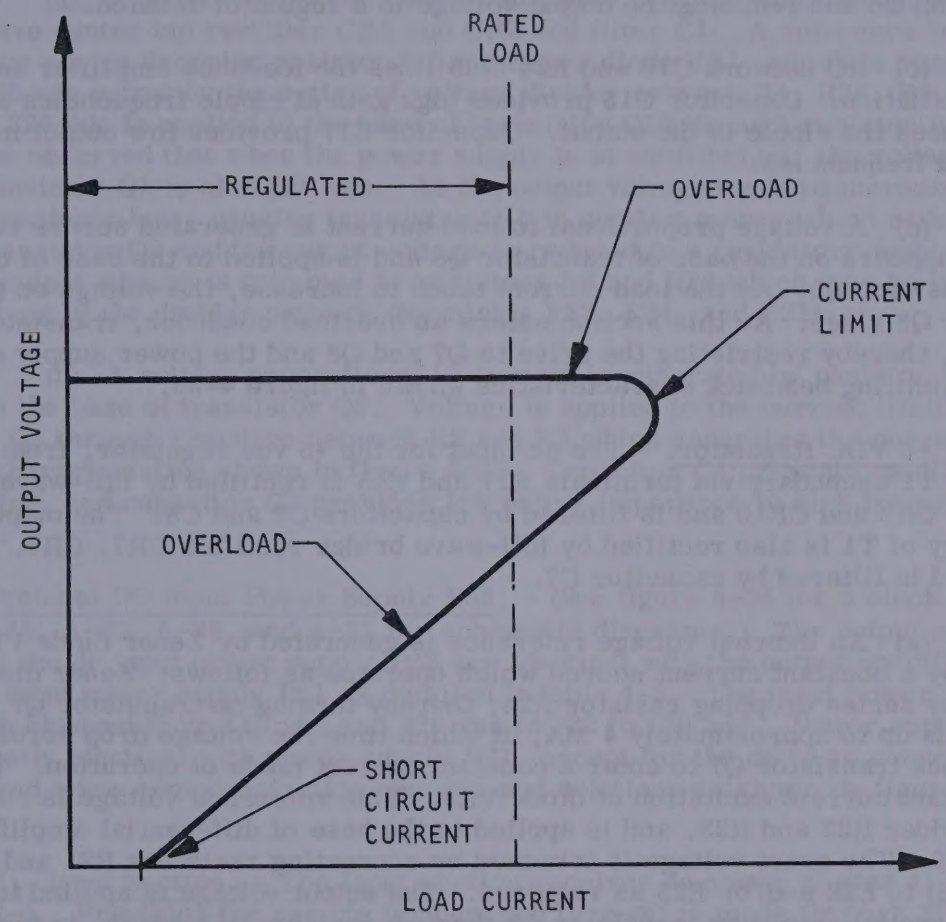


Figure 4-35. – Bendback Short Circuit Protection Characteristics.

(3) -8 VDC Regulator. - The ac input for the -8 vdc regulator, from the transformer secondary via terminals E4 and E6, is rectified by full-wave center tap rectifier CR5 and CR6 and is filtered by capacitors C13 and C14. The positive voltage reference for the +25 vdc regulator, which is generated by Zener diode VR2 is also used as a reference voltage for the -8 vdc regulator.

(a) The -8 VDC output is compared to the +6 VDC reference at the voltage divider R27 and R22. The voltage divider is trimmed up by resistors R25 and R26, which are connected to E35 or E36 as required. Capacitor C15 provides high

frequency by-pass for decreasing ripple, and RC network C16 and R24 stabilizes the loop and determines the transient response.

(b) The voltage divider network R27 and R22 is normally at zero volts when the power supply is at the proper output. It will be noted that the base of differential amplifier transistor Q11 is connected to the zero output and is compared with the negative regulator output by the action of differential amplifier transistors Q10 and Q11. If the output voltage tends to become more negative, transistor Q10 conducts less, causing transistor Q11 to conduct more, thereby reducing the drive to transistors Q7 and Q8 and reducing the output voltage in a regulator fashion.

(c) RC network C16 and R24 stabilizes the feedback amplifier and prevents oscillation. Capacitor C15 provides high gain at ripple frequencies and thereby reduces the ripple in the output. Capacitor C17 provides low output impedance to high frequencies.

(d) A voltage proportional to load current is generated across resistor R21, which appears on the base of transistor Q8 and is applied to the base of current limiting transistor Q9. As the load current tends to increase, the voltage on the base of transistor Q8 rises. As this section enters an overload condition, transistor Q9 is turned on, thereby restricting the drive to Q7 and Q8 and the power supply enters the current limiting bendback characteristics shown in figure 4-35.

(4) +5 VDC Regulator. - The ac input for the +5 vdc regulator, from the transformer T1 secondary via terminals E17 and E18 is rectified by full-wave center tap rectifier CR8 and CR10 and is filtered by capacitors C7 and C8. The output from the secondary of T1 is also rectified by full-wave bridge rectifier CR7, CR8, CR9, and CR10 and is filtered by capacitor C7.

(a) An internal voltage reference is generated by Zener diode VR3 which is actuated by a constant current source which operates as follows: Zener diode VR2 is actuated by series dropping resistor R24, thereby turning on transistor Q7. The current builds up to approximately 4 MA, at which time the voltage drop across resistor R16 causes transistor Q7 to enter a constant current mode of operation. This causes constant current excitation of diode VR3. This reference voltage is reduced by resistive divider R22 and R23, and is applied to the base of differential amplifier transistor Q9. The exact voltage is trimmed by connecting resistors R21 and R20 (E27 and E28) to E22 and/or E23 as required. The output voltage is applied to the base of differential amplifier transistor Q8 through resistor R18 which, in turn, compares the output voltage with the reference. If the output voltage tends to increase, transistor Q8 conducts more heavily, thereby reducing the drive to transistor Q4, pass transistor Q5, and the output voltage is reduced in a regulatory fashion.

(b) RC network CR7 and R25 provides inverse feedback and stabilizes the feedback amplifier. Resistor R27 provides line voltage compensation and decreases ripple. Capacitor C10 provides low output impedance.

(c) A voltage proportional to load current is generated across resistor R14, which appears at the base of transistor Q5 and is applied to the current limiting transistor Q6 through resistive divider R12 and R17, thereby generating the current limiting bendback characteristics shown in figure 4-35.

(5) 230 VDC Regulator. - The ac input for the +230 VDC regulator, from the transformer T1 secondary via terminals E14 and E16, is rectified by full-wave bridge rectifier CR3, CR4, CR5, and CR6 and is filtered by capacitors C2 and C3. The voltage division at capacitors C2 and C3 is guaranteed by the connection between the center tap at secondary S2 and the junction of capacitors C2 and C3. The unregulated voltage at capacitors C2 and C3 is added to the unregulated voltage at capacitor C6.

(a) A boost voltage for control purposes is generated by secondary S1 and full-wave center tap rectifier CR1 and CR2 and filter C1. A reference voltage is generated by series dropping resistor R7 and Zener diode VR1, which is compared with the 220 vdc output by the action of voltage divider network R4, R26, R9, and R10. The 220 vdc is applied to the base of transistor Q10 through resistor R8, and it should be observed that when the power supply is at equilibrium, the voltage on the base of transistor Q1 is also 220 vdc. As the output voltage tends to increase, transistor Q1 conducts less, causing transistor Q10 to conduct more, which reduces the drive to transistor Q2 and the output voltage is reduced in a regulatory fashion. The exact output voltage is trimmed by resistors R9 and R10 which may be included or shorted out of the divider network (terminals E33, E34, and E21).

(b) A voltage proportional to current is generated by resistor R1 and appears on the base of transistor Q2. Voltage is applied to the current limiting transistor Q3 through resistive network R2 and R3 which generates the current limit bendback characteristics shown in figure 4-35. Capacitor C4 prevents oscillation of the regulator, and capacitor C5 provides low output impedance to high frequency transients.

r. Optional DC Input Power Supply PS2. - (See figure 4-36 for a block diagram and figures A-24, A-25, A-26, and A-27 for schematic diagrams.) The output specifications for the dc input power supply PS2 are identical with the output specifications for the ac input power supply PS1 as detailed in table 4-8. The input power specifications are changed from 110 vac and 220 vac to +22 to +30 vdc. Power supply PS2 is electrically identical with power supply PS1, except for the dc to ac converter board A3 and a few component value changes and deletions as shown on figures A-24 and A-25.

(1) Input Section. - The input section receives dc power at pins J1-A (+) and J1-B (−). Provision for remote turn-on and turn-off is made through J2-2 and J2-4. When the receiver FUNCTION switch is in all positions except OFF, these pins are jumpered. This couples dc power through 3 ampere slow-blow fuse F1 to the dc to ac converter A3.

(2) DC to AC Converter PS2A3. - (See figure A-27 for a schematic diagram.) The dc to ac converter PS2A3 is basically an astable multivibrator that oscillates at the rate of approximately 1 kHz. DC power is applied through RFI filter network C1, L1, L2, and C2 to the inverter consisting of transistors Q1 and Q2 and transformers T1 and T2 and their associated components. The application of voltage causes current to flow through resistor R1 into the respective bases of transistors C1 and C2, causing the transistors to initiate conduction. The inverter begins to oscillate through the primary of transformer T1 to the secondary and hence, through resistor R6 to the primary of transformer T2 and to the secondary of T2, thereby turning one transistor on and the other transistor off. The application of voltage from secondary of T2 through resistor R6 applies drive voltage to the primary of saturating transformer T2,

which causes conduction through CR5, R5, T2, and CR3 and the base of transistor Q2, thereby turning Q2 on heavily. Transformer T2 is a self-saturating transformer designed to operate at approximately 1 kHz.

After approximately 500 μsec, the transformer saturation and resistor R6 limits the current, thereby limiting the drive to transistor Q2 and conduction ceases. This initiates a switching action which causes transistor Q1 to turn on heavily and transistor Q2 to turn-off, and the process is repeated at a 1 kHz squarewave rate.

Resistor R4 and diode network CR6 provide back bias during turn-off to transistor Q2, and resistor R3 and CR4 provide similar back-bias on transistor Q1 during turn-on. Diode CR1 prevents reverse polarity across the input and will cause a fuse to blow in that event.

(3) Power Supply Rectification, Filtering and Regulator Circuits. - Refer to paragraphs 4-4q(2) through 4-4q(5).

s. Filters. - Refer to table 4-9 for a listing of the filter subassemblies and their specifications. All the filters are listed except FL19, which is a low-pass filter with the following specifications:

(1) 0 db at 30 MHz

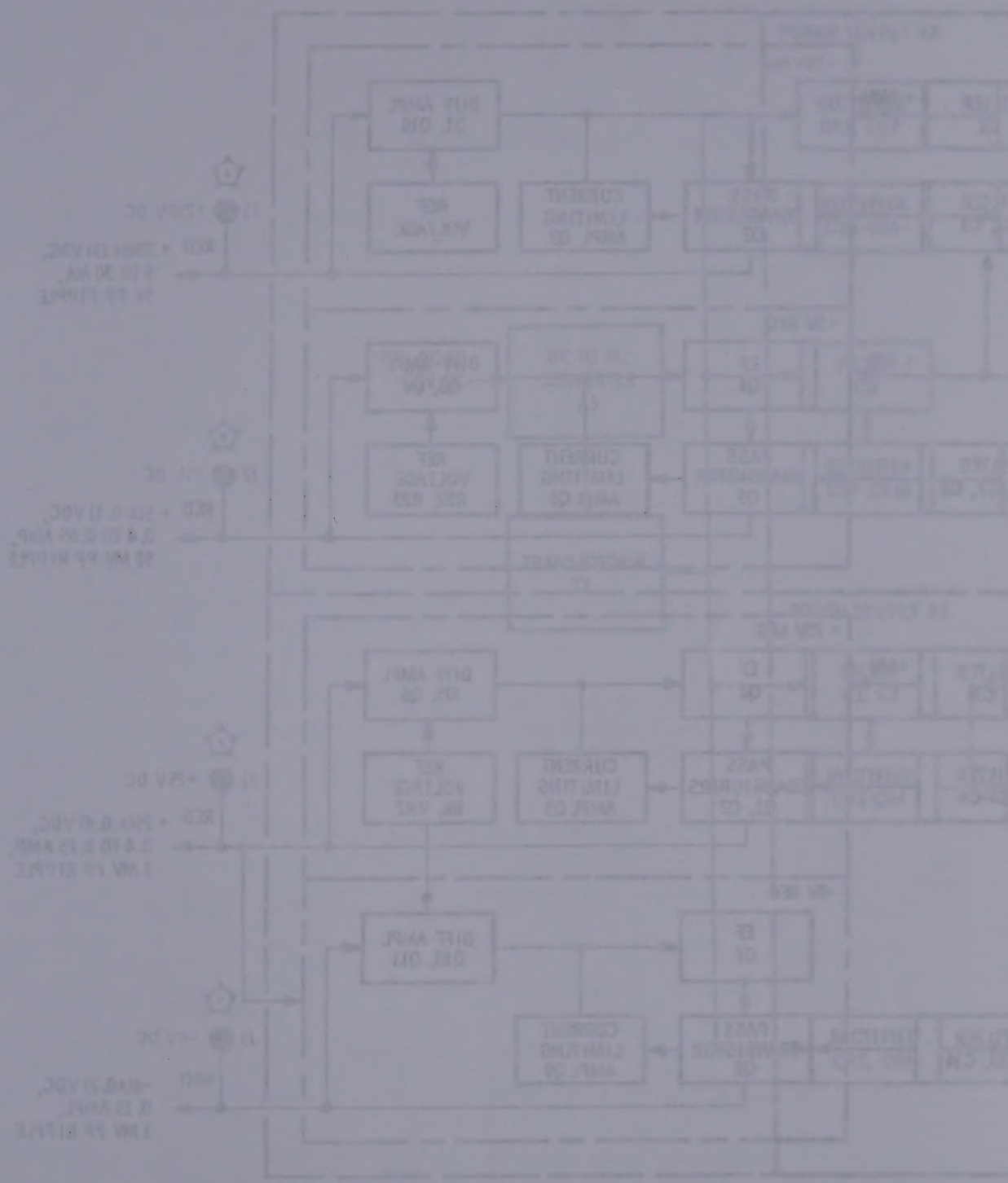
(2) 3 db at 85 MHz

(3) 10 db at 100 MHz

(4) 50 db at 200 MHz

Table 4-9. — Filter Specifications

FILTER	CENTER FREQUENCY	BANDWIDTH
FL1	392 kHz	16 kHz at 1.5 db
FL2	762 kHz	16 kHz at 1.5 db
FL3	2.762 MHz	16 kHz at 1.5 db
FL4	455 kHz	100 Hz at 3 db
FL5	455 kHz	1.0 kHz at 3 db
FL6	455 kHz	2.0 kHz at 3 db
FL7	455 kHz	6 kHz at 3 db
FL8	455 kHz	16 kHz at 1.5 db
FL9	455 kHz	455.250 kHz max to 461.100 kHz min at 3 db
FL10	455 kHz	448.900 kHz max to 454.750 kHz min at 3 db
FL21 (Optional)	455 kHz	3.5 kHz at 3 db
FL22 (Optional)	455 kHz	3.0 kHz min to 3.5 kHz max at 3 db. Note: - Precision delay time of ±25 μsec.



which causes conduction through CR5, R5, T2, and CR3 and the base of transistor Q2, thereby turning Q2 on heavily. Transformer T2 is a self-saturating transformer designed to operate at approximately 1 kHz.

After approximately 500 μsec, the transformer saturation and resistor R6 limits the current, thereby limiting the drive to transistor Q2 and conduction ceases. This initiates a switching action which causes transistor Q1 to turn on heavily and transistor Q2 to turn-off, and the process is repeated at a 1 kHz squarewave rate.

Resistor R4 and diode network CR6 provide back bias during turn-off to transistor Q2, and resistor R3 and CR4 provide similar back-bias on transistor Q1 during turn-on. Diode CR1 prevents reverse polarity across the input and will cause a fuse to blow in that event.

(3) Power Supply Rectification, Filtering and Regulator Circuits. - Refer to paragraphs 4-4q(2) through 4-4q(5).

s. Filters. - Refer to table 4-9 for a listing of the filter subassemblies and their specifications. All the filters are listed except FL19, which is a low-pass filter with the following specifications:

(1) 0 db at 30 MHz

(2) 3 db at 85 MHz

(3) 10 db at 100 MHz

(4) 50 db at 200 MHz

Table 4-9. — Filter Specifications

FILTER	CENTER FREQUENCY	BANDWIDTH
FL1	392 kHz	16 kHz at 1.5 db
FL2	762 kHz	16 kHz at 1.5 db
FL3	2.762 MHz	16 kHz at 1.5 db
FL4	455 kHz	100 Hz at 3 db
FL5	455 kHz	1.0 kHz at 3 db
FL6	455 kHz	2.0 kHz at 3 db
FL7	455 kHz	6 kHz at 3 db
FL8	455 kHz	16 kHz at 1.5 db
FL9	455 kHz	455.250 kHz max to 461.100 kHz min at 3 db
FL10	455 kHz	448.900 kHz max to 454.750 kHz min at 3 db
FL21 (Optional)	455 kHz	3.5 kHz at 3 db
FL22 (Optional)	455 kHz	3.0 kHz min to 3.5 kHz max at 3 db. Note: - Precision delay time of ±25 μsec.

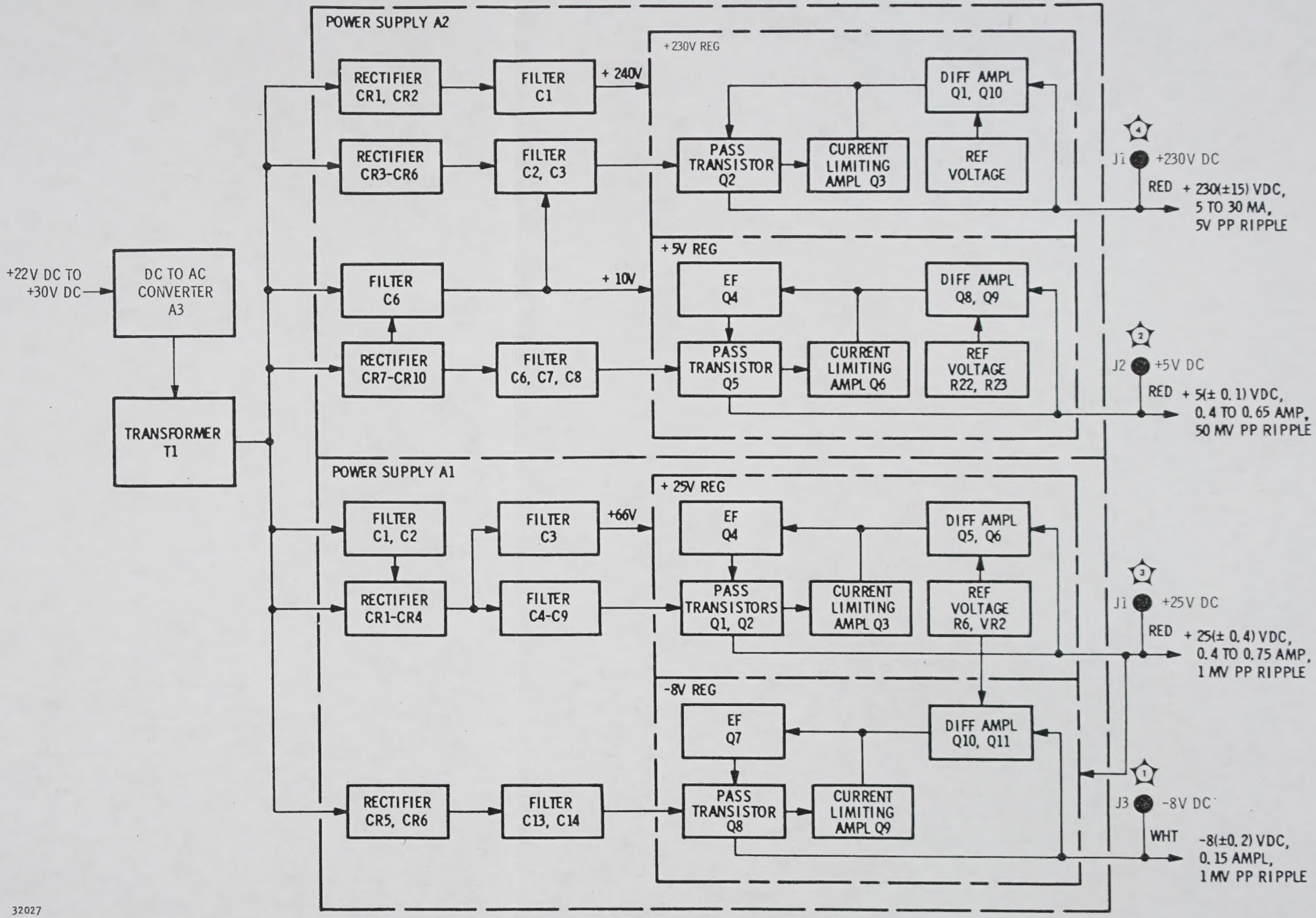


Figure 4-36. – Power Supply PS2, Block Diagram.

CHAPTER 5

PREVENTIVE MAINTENANCE

5-1. GENERAL. - This chapter provides information needed for periodic preventive maintenance and inspection of the receiver.

WARNING

HIGH VOLTAGE (SPECIFICALLY +230 VDC) IS PRESENT AT OUTPUT OF POWER SUPPLY PS1 AND IN COUNTER A9. EITHER DISCONNECT POWER OR BE EXTREMELY CAUTIOUS WHEN WORKING ON RECEIVER WITH THE DUST AND RFI COVERS REMOVED. CONTACT WITH THIS VOLTAGE COULD RESULT IN INJURY TO PERSONNEL.

5-2. PREVENTIVE MAINTENANCE EQUIPMENT. - Table 5-1 lists all test equipment required during the performance of the maintenance procedures in this chapter. Test equipment equivalent to those listed in the table or test equipment with sufficient capabilities to conduct the test, may be substituted.

Note: – If a 50 to 75 ohm matching transformer is not available for connection between test equipment and the LOW IMPD ANT input to the receiver, allow for 5 db differences in the output indications of the receiver.

Table 5-1. – Preventive Maintenance Test Equipment.

		EQUIVALENT STANDARD MILITARY EQUIPMENT			
COMMON NAME	PART/ MODEL NO.	NOMENCLATURE	FSN	TECHNICAL MANUAL OR ORDER	QTY
AC Voltmeter	Hewlett-Packard Model 400E	AN/USM-265 OR MIL-V-9999	6625-995-7716 6625-724-4111	TM11-6625-320-12 33A1-12-349-31	2
Attenuator (1 db steps)	Hewlett-Packard Model 355C	–	5985-993-1377	33A1-13-140-1	1
Attenuator (10 db steps)	Hewlett-Packard Model 355D	–	5985-957-1860	33A1-13-140-1	1
Audio Generator	Hewlett-Packard Model 206A	–	–	–	
DC Voltmeter	Hewlett-Packard Model 410B	ME-26( )/U	6625-360-2493	TM11-6625-200 33A1-12-98-21	1

Table 5-1. – Preventive Maintenance Test Equipment -Continued.

		EQUIVALENT STANDARD MILITARY EQUIPMENT			
COMMON NAME	PART/ MODEL NO.	NOMENCLATURE	FSN	TECHNICAL MANUAL OR ORDER	QTY
Matching Transformer (50 to 95 ohms)	Anzac Model TDN-5350 (old TP-75)	—	—	—	1
Resistor	600 ohm, 1/2 w, carbon	—	—	—	2
RF Voltmeter	Millivac MV-928A	AN/URM-145	6625-973-3980	TM11-6625-524-14	1
			6625-880-1576	33A1-12-798-1	
RF Random Noise Generator	Aerospace Research NS-LB	—	6625-461-5938	—	1
Signal Generator	Hewlett-Packard Model 545B	AN/GRM-50	6625-973-3986	TM11-6625-573-15	1
			6625-494-856YA	33A1-8-599-1	1
Oscilloscope	Tektronix Model 453	MIL-O-9960C	6625-892-5251	33A1-13-336-11	1

5-3. SCHEDULE FOR PERIODIC MAINTENANCE. - Perform periodic maintenance on a scheduled basis as detailed in table 5-2.

Table 5-2. – Recommended Maintenance Schedule.

FUNCTION	PARAGRAPH NUMBER	CONTINUOUS OPERATION	STANDBY OPERATION
Visual Inspection	5-5	Every 3 months	As required by maintenance supervisor
Cleaning	5-6	Every 3 months	As required by maintenance supervisor
Lubrication	5-7	As required by maintenance supervisor	As required by maintenance supervisor
Performance Check	5-8	Every 3 months	As required by maintenance supervisor

5-4. PURPOSE OF PREVENTIVE MAINTENANCE. - Preventive or scheduled maintenance is defined as those measures taken periodically, or when needed, to achieve maximum efficiency in performance, to ensure continuity of service, to reduce major breakdowns, and to lengthen the useful life of equipment or system. This form of maintenance, for the receiver, consists principally of cleaning and periodic inspections, including minimum performance tests.

a. Inspections. - Inspections fall into two main categories. First, there is the regular visual inspection of the mechanical aspects of the receiver, which is conducted for the purpose of finding dirt, corrosion, loose connections, mechanical defects, and other sources of trouble. Second, there are the functional inspections that are accomplished through periodic performance tests. To realize optimum results from the regular functional inspections, keep a careful record of the performance data on each receiver. Comparison of data taken on a particular equipment at different times reveals slow, progressive drifts that may be too small to show up significantly in any one test. Any marked variations should be regarded as abnormal, and should be investigated immediately.

b. Cleaning. - Cleaning of the internal electronic components and subassemblies should be held to the absolute minimum and should only be performed as needed. Unnecessary cleaning can sometimes disturb the internal components and cause performance degradation or a malfunction when the receiver would otherwise be operating properly. Cleaning of outer surfaces should be periodically performed to maintain acceptable appearance.

5-5. VISUAL INSPECTION. - Visually inspect receiver for physical damage to panels, controls, cables, and connectors. If damage is evident, replace or repair defective components. Check knobs, switches, connectors, handles, and features for looseness or mechanical discrepancies.

5-6. CLEANING. Use a vacuum source and a soft-bristled brush to clean the internal electrical parts of the receiver. Use the vacuum source to remove loose dirt from the electrical parts. Use a soft-bristled brush to loosen dirt which remains after vacuuming, then vacuum again. When cleaning the receiver external surfaces, use a soft, clean cloth to wipe dust, grease, or other foreign matter from the surface.

WARNING

ENSURE THAT ALL POWER IS REMOVED FROM THE RECEIVER PRIOR TO CLEANING. INJURY TO PERSONNEL COULD RESULT FROM CONTACT WITH EXPOSED ELECTRICAL CONNECTIONS.

CAUTION. – Use a nonconductive, soft-bodied cleaning attachment on vacuum source, and exercise care in manipulating the attachment within the equipment to prevent damage to fragile parts.

5-7. LUBRICATION. - This receiver requires the minimum of lubricant when used in a clean environment. In general, do not accomplish lubrication unless the switch or tuning control becomes stiff or rough in operation.

WARNING

CLEANING SOLVENTS ARE FLAMMABLE AND TOXIC. KEEP AWAY FROM OPEN FLAME OR HOT SURFACES. TAKE CARE NOT TO INHALE THE TOXIC FUMES. AVOID PROLONGED CONTACT WITH THE SKIN.

CAUTION. – Do not use cleaning solvents on plastic, rubber parts, or treated coils. Never use a chemical solvent on the electrical contacts of switches, relays, or connectors.

a. Tuner Subassembly A21. - Lubrication of the tuner subassembly gears can be accomplished while it is installed in the receiver.

CAUTION. – The tuner subassembly A21 is a high precision tuning capacitor, therefore all maintenance must be accomplished with great care. Do not disassemble in the field.

(1) Remove bottom dust cover from receiver.

(2) Remove three mounting screws and remove bottom cover (see figure 1-3) from tuner subassembly gear box.

(3) If gear box (see figure 5-1) is dirty, clean shafts and gears using cleaning solvent conforming to Federal Specification P-S-661.

(4) After gear box has been cleaned, or if gear box is not dirty, apply a small quantity (quantity to be determined by maintenance supervisor) of grease conforming to MIL-G-23827 (or equivalent) to the gear teeth.

(5) Replace the tuner and receiver dust covers.

b. Band Change Gear Box MP1. - The band change gear box (MP1, figure 5-2) must be removed from the receiver to accomplish lubrication. Refer to paragraph 6-8g in Chapter 6 for removal instructions.

(1) Remove four mounting screws and remove cover from gear box.

(2) If gear box requires cleaning, clean shafts and gears (see figure 5-2) using cleaning solvent conforming to Federal Specification P-S-661.

(3) After gear box has been cleaned, or if gear box is not dirty, apply a small quantity (to be determined by maintenance supervisor), of grease conforming to MIL-G-23827 (or equivalent) to the gear teeth.

(4) Replace the gear box cover and install gear box in receiver.

5-7. LUBRICATION. - This receiver requires the minimum of lubricant when used in a clean environment. In general, do not accomplish lubrication unless the switch or tuning control becomes stiff or rough in operation.

WARNING

CLEANING SOLVENTS ARE FLAMMABLE AND TOXIC. KEEP AWAY FROM OPEN FLAME OR HOT SURFACES. TAKE CARE NOT TO INHALE THE TOXIC FUMES. AVOID PROLONGED CONTACT WITH THE SKIN.

CAUTION. – Do not use cleaning solvents on plastic, rubber parts, or treated coils. Never use a chemical solvent on the electrical contacts of switches, relays, or connectors.

a. Tuner Subassembly A21. - Lubrication of the tuner subassembly gears can be accomplished while it is installed in the receiver.

CAUTION. – The tuner subassembly A21 is a high precision tuning capacitor, therefore all maintenance must be accomplished with great care. Do not disassemble in the field.

(1) Remove bottom dust cover from receiver.

(2) Remove three mounting screws and remove bottom cover (see figure 1-3) from tuner subassembly gear box.

(3) If gear box (see figure 5-1) is dirty, clean shafts and gears using cleaning solvent conforming to Federal Specification P-S-661.

(4) After gear box has been cleaned, or if gear box is not dirty, apply a small quantity (quantity to be determined by maintenance supervisor) of grease conforming to MIL-G-23827 (or equivalent) to the gear teeth.

(5) Replace the tuner and receiver dust covers.

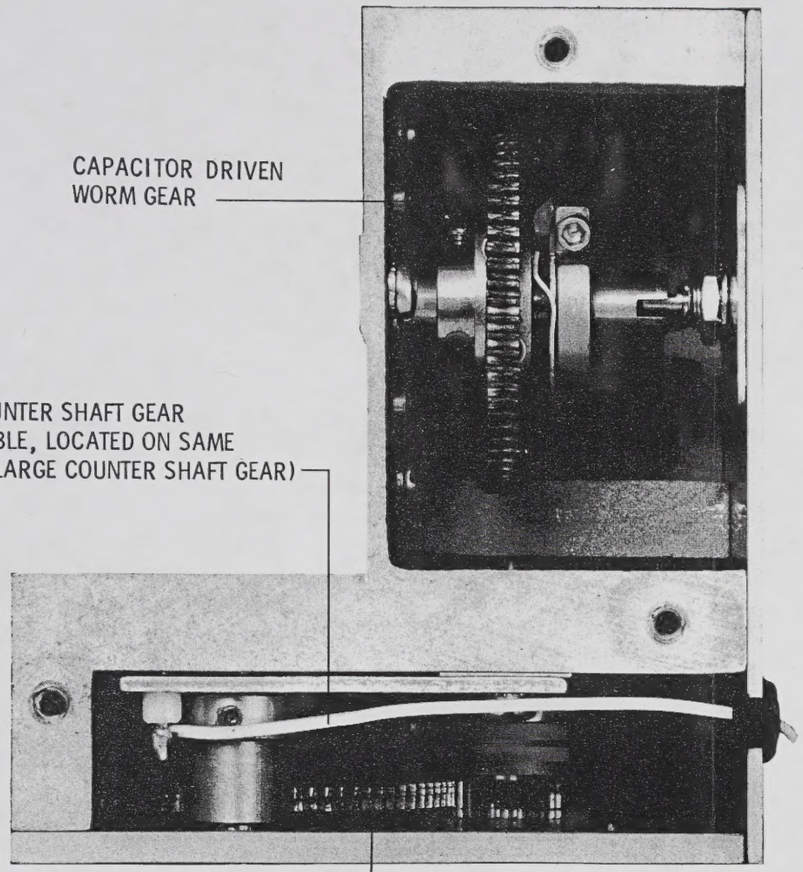
b. Band Change Gear Box MP1. - The band change gear box (MP1, figure 5-2) must be removed from the receiver to accomplish lubrication. Refer to paragraph 6-8g in Chapter 6 for removal instructions.

(1) Remove four mounting screws and remove cover from gear box.

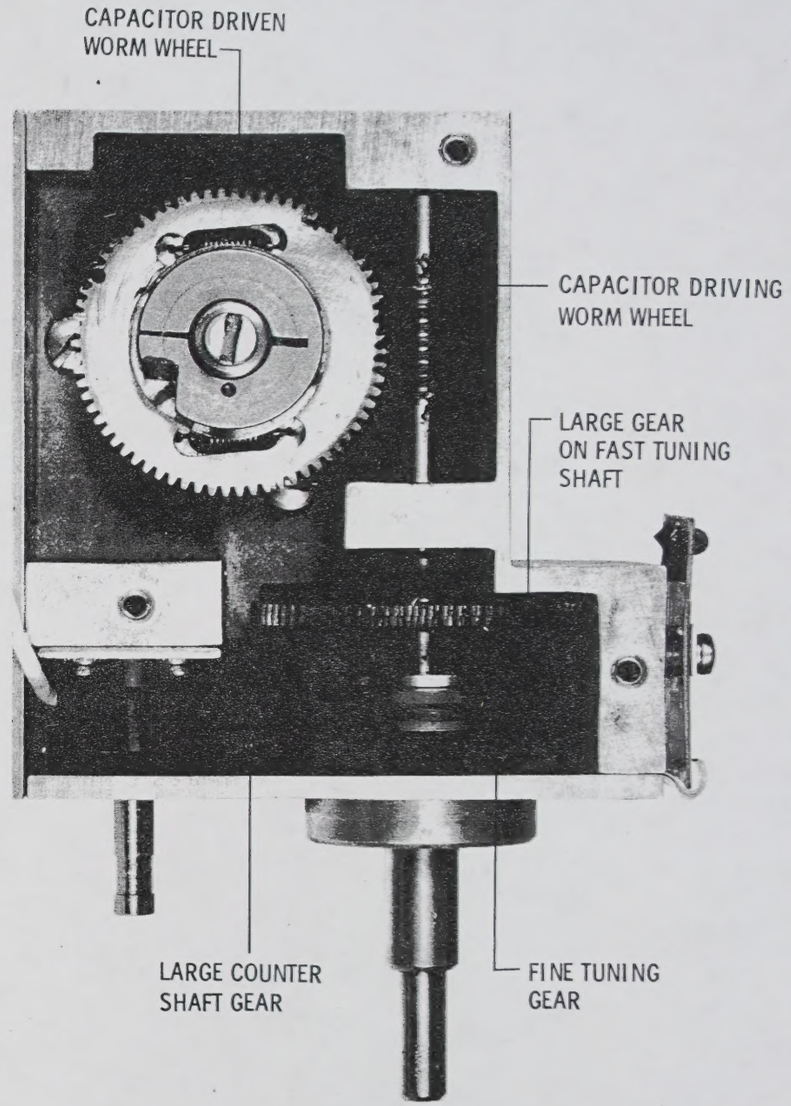
(2) If gear box requires cleaning, clean shafts and gears (see figure 5-2) using cleaning solvent conforming to Federal Specification P-S-661.

(3) After gear box has been cleaned, or if gear box is not dirty, apply a small quantity (to be determined by maintenance supervisor), of grease conforming to MIL-G-23827 (or equivalent) to the gear teeth.

(4) Replace the gear box cover and install gear box in receiver.



BOTTOM VIEW



SIDE VIEW

32054
70042027/70081006

Figure 5-1. – Tuner Subassembly Gear Box.

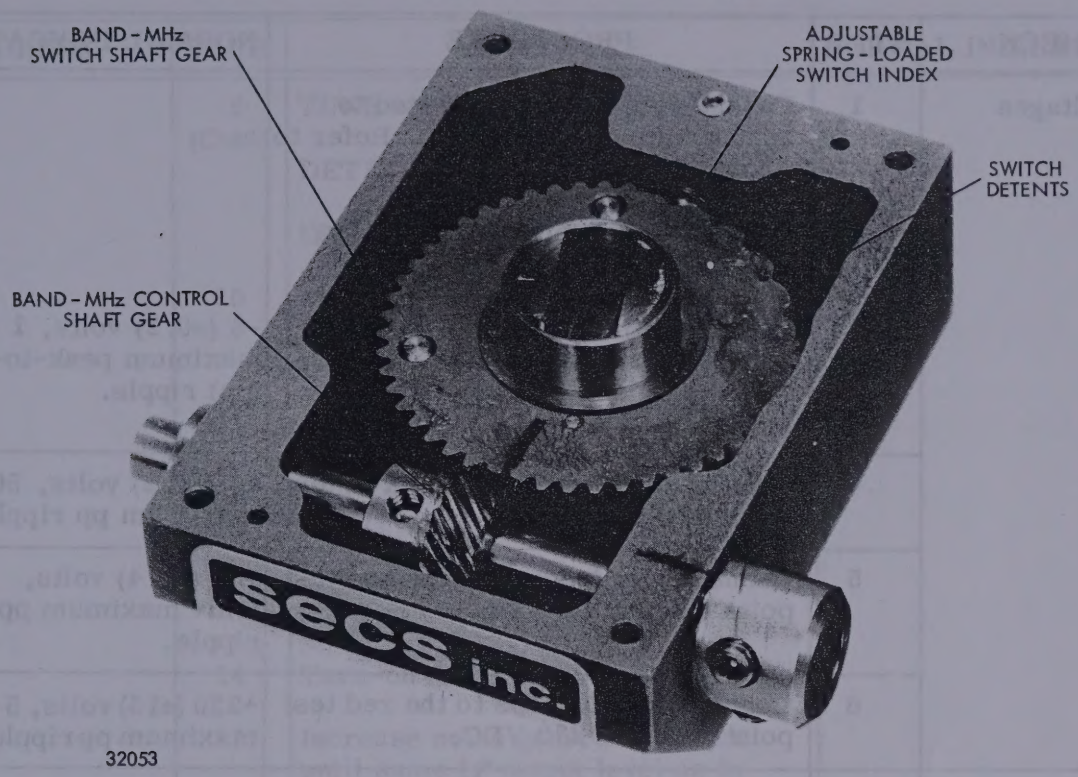


Figure 5-2. – Band Change Gear Box MP1.

c. Rotary Switches. - The rotary switches may be cleaned and lubricated while installed in receiver.

CAUTION. – When cleaning the rotary switches, be careful to avoid bending any part of the switch contact.

Do not use a chemical solvent on the switch contacts to avoid damage to equipment.

Do not use abrasives or burnishes on the switch contacts. Damage to the plating of the electrical contacts could cause receiver to malfunction.

(1) Clean the switch contacts and detents with a vacuum source first to remove loose dirt. Use a soft-bristled brush to loosen dirt which remains after vacuuming, then vacuum again.

(2) Apply a small quantity (quantity to be determined by maintenance supervisor) of grease conforming to MIL-G-23827 to the switch detents and contacts.

5-8. PERFORMANCE CHECK. - The performance testing that is required on a scheduled basis (every three months) is provided in table 5-3.

Table 5-3. – Performance Check.

CHECK	STEP	PROCEDURE	NORMAL INDICATION
DC voltages	1	Ensure receiver is connected to appropriate power source. Refer to Chapter 2.	
	2	Remove top cover from receiver, exposing power supply test points.	
	3	Connect oscilloscope to the white test point labeled -8 VDC. Use black test point labeled OV for ground connection.	-8 (±0.2) volts, 1 mv maximum peak-to-peak (pp) ripple.
	4	Connect oscilloscope to the red test point labeled +5 VDC.	+5 (±0.2) volts, 50 mv maximum pp ripple.
	5	Connect oscilloscope to the red test point labeled +25 VDC.	+25 (±0.4) volts, 1 mv maximum pp ripple.
	6	Connect oscilloscope to the red test point labeled +230 VDC.	+230 (±15) volts, 5 volts maximum pp ripple.
Noise figure (noise generator method)	7	Connect equipment as shown in figure 5-3.	
	8	Turn-on receiver and RF voltmeter.	
	9	Adjust receiver controls as follows: BAND-MHZ switch: 1.5-2.7 MHz LOCK-UNLOCK control: UNLOCK FUNCTION switch: MGC AUDIO GAIN control: WIDE ANTENNA TRIM control: OFF DIV-TUNE ANT DSBL switch: OFF RF GAIN control: MAX FINE TUNE control: 0, mid-position	

Table 5-3. – Performance Check - Continued.

CHECK	STEP	PROCEDURE	NORMAL INDICATION
	9 (Cont)	TUNE control: 2.0 MHz DETECTOR switch: AM IF BANDWIDTH: 6 kHz	
	10	Adjust noise generator output to lowest level. Be sure that noise generator is OFF.	
	11	Adjust attenuator to 0 db.	
	12	Record the IF output voltage from the RF voltmeter.	
	13	Adjust attenuator to 3 db of attenuation.	
	14	Turn-on noise generator.	
	15	Increase noise generator output until same IF output level as in step 12 is again obtained.	
	16	Record noise figure directly from face of noise generator meter.	Must not exceed 10 db.
	17	Repeat steps 10 through step 16 for the following BAND-MHZ switch and TUNE control adjustments: BAND MHZ: TUNE: 2.7-5 MHz 4.0 MHz 5-9 MHz 7.0 MHz 9-17 MHz 12.0 MHz 17-32 MHz 24.0 MHz	Same as for step 16.
Sensitivity (Alternate for noise figure check)	18	Connect equipment as shown in figure 5-4.	
	19	Turn-on receiver and RF voltmeter.	

Table 5-3. – Performance Check - Continued.

CHECK	STEP	PROCEDURE	NORMAL INDICATION
	20	Adjust receiver controls as follows: BAND-MHZ switch: 1.5-2.7 LOCK-UNLOCK control: UNLOCK TUNE control: 2.0 MHz FUNCTION switch: MGC NAR-WIDE control: WIDE ANTENNA TRIM control: OFF DIV TUNE-ANT DSBL switch: OFF RF GAIN control: MAX FINE TUNE control: 0, mid-position BFO KHZ 0, mid-position DETECTOR switch: AM IF BANDWIDTH: 6 kHz NOISE LIMITER control: OFF AUDIO GAIN control: MAX LINE GAIN control: MAX	
	21	Tune receiver to 2 MHz and set signal generator power output to minimum.	
	22	Read and record IF noise output as indicated on RF voltmeter.	
	23	Set signal generator output frequency to approximately 2 MHz at 10 μv, then adjust signal generator	

Table 5-3. – Performance Check - Continued.

CHECK	STEP	PROCEDURE	NORMAL INDICATION
	23 (Cont)	frequency for maximum IF output as indicated on RF voltmeter.	
	24	Decrease signal generator output to an IF output level 10 db above the level obtained in step 22.	
	25	Read and record signal generator power output.	Should be 5 μv or less
	26	Repeat steps 21 through 25 for the following BAND-MHZ switch and TUNE control settings (and signal generator frequencies): BAND-MHZ switch — TUNE control 2.7-5 — 4.0 MHz 5-9 — 7.0 MHz 9-17 — 12.0 MHz 17-32 — 24.0 MHz	Same as for step 25
Overall gain	27	Connect equipment as shown in figure 5-5.	
	28	Turn-on receiver and test equipment.	
	29	Adjust receiver controls as follows: BAND-MHZ: 1.5-2.7 MHz LOCK-UNLOCK: UNLOCK DETECTOR: AM IF BANDWIDTH: 6 kHz NOISE LIMITER: MIN LINE GAIN: MAX TUNE: 2.0 MHz FUNCTION: MGC ANTENNA TRIM: OFF DIV TUNE-ANT DSBL: OFF AUDIO GAIN: MAX RF GAIN: MAX	
	30	Tune the signal generator to 2.0 MHz cw.	

Table 5-3. – Performance Check - Continued.

CHECK	STEP	PROCEDURE	NORMAL INDICATION
	31	Adjust the signal generator output for a detector output voltage of +2 (±0.05) volts as indicated on the dc voltmeter.	
	32	Record the signal generator output level (in dbm).	Approximately -100 dbm
	33	Repeat steps 31 and 32 for the following BAND-MHZ switch and TUNE control settings (and signal generator frequencies): BAND-MHZ switch — TUNE control 2.7-5 — 4.0 MHz 5-9 — 7.0 MHz 9-17 — 12.5 MHz 17-32 — 24.0 MHz	
	34	Compare results of step 32 for all five frequencies.	Variation in signal generator output levels must not exceed 10 db.
	35	Adjust signal generator to the test frequency that caused the highest signal generator input level.	
	36	Set signal generator output to -99 dbm, with 30 percent modulation at 400 Hz.	
	37	Tune the receiver for maximum IF response.	
	38	Record the line audio power shown on AC voltmeter connected to LINE OUT CH A terminals (TB1-4 and TB1-5).	Should be equal to or greater than 0 dbm (0.755 volt).
	39	Record the phone audio power shown on AC voltmeter connected to PHONE AUDIO OUT terminal TB1-8.	Should be equal to or greater than +17 dbm (5.5 volts).
	40	Turn-off the signal generator modulation (cw mode).	

Table 5-3. – Performance Check - Continued.

CHECK	STEP	PROCEDURE	NORMAL INDICATION
	41	Record the IF output level shown on the RF voltmeter.	Should be greater than -21 dbm (20 mv).
	42	Set the signal generator output (still unmodulated) to 7.0 MHz and -99 dbm 2.5μv.	
	43	Tune the receiver for maximum IF output power as shown on RF voltmeter and record receiver frequency.	
	44	Reduce receiver RF gain until IF output voltage is 20 mv as shown on RF voltmeter.	
	45	Increase signal generator output to -79 dbm.	
	46	Record IF output voltage as shown on RF voltmeter.	200 (±20) mv
	47	Set receiver AUDIO GAIN control to MAX.	
	48	Set receiver LINE GAIN control and RF GAIN control to MAX.	
	49	Set DETECTOR switch to LSB.	
	50	Tune the receiver to receiver frequency recorded in step 43 plus 0.001 MHz.	
	51	Adjust signal generator output to obtain 0 dbm on AC voltmeter connected to LINE OUT CH A terminals (TB1-4 and TB1-5).	
	52	Record signal generator output level.	Should be less than -99 dbm.
	53	Connect AC voltmeter to PHONE AUDIO OUT terminal TB1-8 on the rear panel.	

Table 5-3. – Performance Check - Continued.

CHECK	STEP	PROCEDURE	NORMAL INDICATION
	54	Adjust signal generator output level for +17 dbm as indicated on AC voltmeter connected to PHONE AUDIO OUT terminal TB1-8.	
	55	Record signal generator output level.	Should be less than -99 dbm.
	56	Set DETECTOR switch to USB.	
	57	Tune the receiver to receiver frequency recorded in step 43 minus 0.001 MHz.	
	58	Repeat steps 51 through 55.	Same as for steps 51 through 55.
	59	Set DETECTOR switch to CW, and IF BANDWIDTH switch to 6.	
	60	Adjust BFO KHZ control to +1 or -1 KHZ. Retune receiver maximum indication on RF voltmeter connected to IF OUT J6.	
	61	Repeat steps 51 through 55.	Same as for steps 51 through 55.

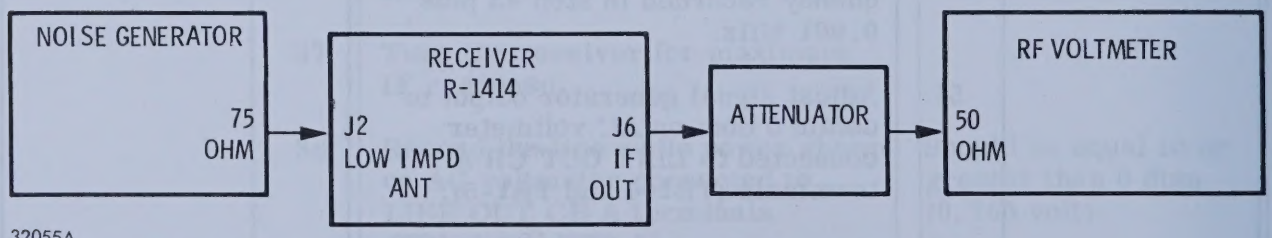


Figure 5-3. – Noise Figure, Test Setup Diagram.

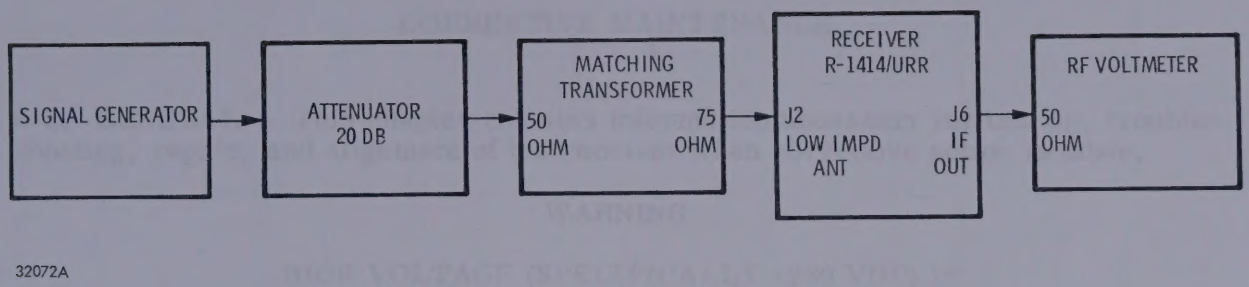


Figure 5-4. – Sensitivity Check, Test Setup Diagram.

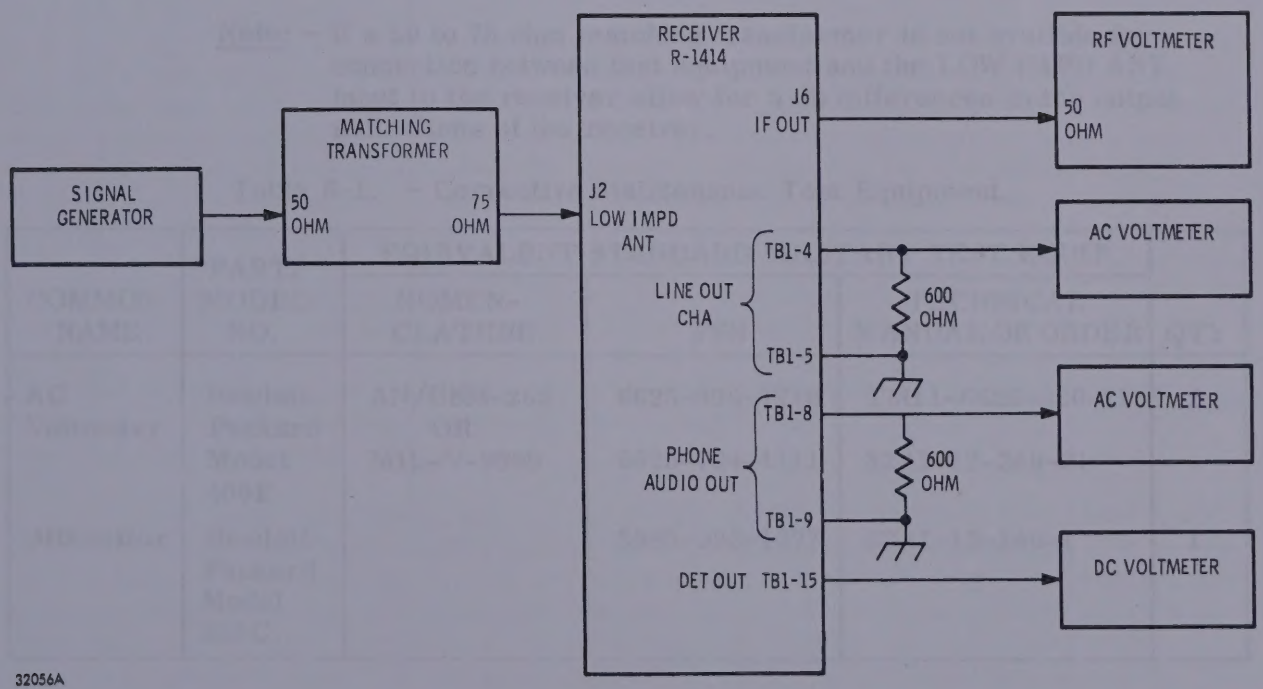


Figure 5-5. – Overall Gain, Test Setup Diagram.

CHAPTER 6

CORRECTIVE MAINTENANCE

6-1. GENERAL. - This chapter contains information necessary for testing, troubleshooting, repair, and alignment of the receiver when corrective action is taken.

WARNING

HIGH VOLTAGE (SPECIFICALLY +230 VDC) IS PRESENT AT OUTPUT OF POWER SUPPLY PS1 AND IN COUNTER A9. EITHER DISCONNECT POWER OR BE EXTREMELY CAUTIOUS WHEN WORKING ON RECEIVER WITH THE DUST AND RFI COVERS REMOVED. CONTACT WITH THIS VOLTAGE COULD RESULT IN INJURY TO PERSONNEL.

6-2. CORRECTIVE MAINTENANCE TEST EQUIPMENT. - A list of test equipment required for testing, alignment, and troubleshooting the receiver is provided in table 6-1. Test equipment equivalent to those listed in the table or test equipment with sufficient capabilities to conduct the test, may be substituted.

Note: – If a 50 to 75 ohm matching transformer is not availble for connection between test equipment and the LOW IMPD ANT input to the receiver allow for 5 db differences in the output indications of the receiver.

Table 6-1. – Corrective Maintenance Test Equipment.

COMMON NAME	PART/ MODEL NO.	EQUIVALENT STANDARD MILITARY TEST EQUIP.			QTY
		NOMEN-CLATURE	FSN	TECHNICAL MANUAL OR ORDER	
AC Voltmeter	Hewlett-Packard Model 400E	AN/USM-265 OR MIL-V-9999	6625-995-7716 6625-724-4111	TM11-6625-320-12 33A1-12-349-31	2
Attenuator	Hewlett-Packard Model 355C	—	5985-993-1377	33A1-13-140-1	1

Table 6-1. – Corrective Maintenance Test Equipment - Continued.

COMMON NAME	PART MODEL NO.	EQUIVALENT STANDARD MILITARY TEST EQUIP.			QTY
		NOMEN-CLATURE	FSN	TECHNICAL MANUAL OR ORDER	
Attenuator	Hewlett Packard Model 355D	-	5985-957-1860	33A1-13-140-1	1
Audio Generator	Hewlett Packard Model 206A	-	-	-	1
DC Voltmeter	Hewlett Packard Model 410B	ME-26( )/U	6625-360-2493	TM11-6625-200 33A1-12-98-21	1
Headset	Telephonics Model 165A	-	-	-	1
Frequency Counter	Hewlett Packard Model 5245L	MIL-C-9988 Type 1	6625-014-6057	33A1-10-76-1	1
Isolation Trans-former	-	-	9950-356-1779	-	1
Matching Trans-former (50 to 75 ohms)	Anzac Model TDN-5350 (old TP-75)	-	-	-	1
Resistor	600 ohms, 1/2 w, carbon	RC20GF601J	-	-	2
RF Voltmeter	Millivac MV-928A	AN/URM-145	6625-973-3986 6625-880-1576	TM11-6625-524-14 33A1-12-798-1	1
RF Random Noise Generator	Aerospace Research NS-LB	-	6625-461-5938	-	1

Table 6-1. – Corrective Maintenance Test Equipment - Continued.

COMMON NAME	PART MODEL NO.	EQUIVALENT STANDARD MILITARY TEST EQUIP.			QTY
		NOMEN-CLATURE	FSN	TECHNICAL MANUAL OR ORDER	
Signal Generator	Hewlett-Packard Model 545B	AN/GAM-50	6625-973-3986 6625-494-8565YA	TM11-6625-513-15 33A1-8-599-1	1 1
Sweep Generator	Telonic SM-2000	—	—	—	1
Oscil-loscope	Tektronic Model 453	MIL-O-9960C	6625-892-5251	33A1-13-336-11	1

6-3. GENERAL TESTING INFORMATION. - This receiver contains solid state components. Ensure that equipment, soldering irons, and other items are isolated from their power input circuits. A suitable isolation transformer, as identified by FSN 9950-356-1779 (or equivalent) should be used when required. Never connect test equipment (other than multimeters and VTVMs) outputs directly to a transistor circuit; use a coupling capacitor. Make test equipment connections with care so that shorts will not be caused by exposed test equipment connectors.

a. Test Points. - The receiver is equipped with test points for connection of test equipment. The test points should be used whenever possible to avoid needless disassembly of equipment. These test points are shown on the receiver block diagram (see figure 4-1) in Chapter 4 and on the schematic diagrams that are located in Appendix A. Paragraph 6-4 provides a table which lists these test points and the expected voltages or waveforms.

b. Voltage Measurements. - This equipment is transistorized. When measuring voltages, use tape or sleeving (spaghetti) to insulate the entire test probe, except for the extreme tip. A momentary short circuit can ruin the transistor. Use the same or equivalent dc voltmeter specified in the test equipment list. Refer to table 6-2 for a listing of the transistor bias voltages and to figure A-1 for transistor base terminal diagrams.

c. Resistance Measurements. - Before using any ohmmeter to test transistors or circuits, check the open circuit voltage across the ohmmeter test leads. Do not use the ohmmeter if its open-circuit voltage exceeds 1.5 volts. Also, since the RX1 range normally connects the ohmmeter internal battery directly across the test leads, the comparatively high current (50 ma or more) may damage the transistor under test. As a general rule it is not recommended that the RX1 range of any ohmmeter be used when testing low-power transistors.

d. Intermittant Troubles. - In all of the tests, the possibility of intermittent troubles should not be overlooked. If present, this type of trouble often may be made to appear by lightly tapping the equipment. Make a visual inspection of the wiring and connections. Minute cracks in printed circuit boards or broken solder connections can cause intermittent operation. A magnifying glass is often helpful in locating defects in printed boards. Continuity measurements of printed conductors may be made using the same technique ordinarily used on conventional wiring; observe ohmmeter precautions in paragraph 6-3c.

e. Transistor Testing. - Transistors are soldered in the circuit. Every effort should be made to troubleshoot the equipment without physically unsoldering and removing the transistors. When measuring resistance of circuit elements connected across the junction of any transistor (base-emitter or base-collector) consider polarity of the ohmmeter and try measurements with the ohmmeter connected one way and then reverse the leads. Also consider that different values of resistance will be obtained with the ohmmeter on different ranges. As an example, if the transistor junction or a resistor plus the transistor junction is measured in the forward direction on the RX10 range, the actual reading will be less than if taken with the ohmmeter on the RX100 range. When in doubt about the result of resistance measurements, check known good equipment for correct readings. Perform as many in-circuit tests as practical before removing wired-in transistors for checking with a transistor tester.

Table 6-2. – Transistor Bias Voltages

SUBASSEMBLY	TRANSISTOR	+VDC		
		E	B	C
RF Amplifier A3	Q1	12.0	11.5	7.1
	Q2	6.5	7.1	12.0
	Q3	12.0	11.5	7.1
	Q4	6.5	7.1	12.0
	Q5 (A3 ON)	24.3	24.9	24.3
	Q5 (A3 OFF)	0.0	0.0	24.5
	Q6 (A3 ON)	25.0	24.3	24.3
	Q6 (A3 OFF)	25.0	24.5	0.0
First Mixer A6	Q5	12.0	11.5	4.8
	Q6	4.1	4.8	12.0
First Local Oscillator A7A1	Q1	19.0	19.5	24.0
	Q2	18.5	19.0	24.0
	Q3	5.9	6.5	18.0
	Q4	18.5	19.0	24.5

Table 6-2. – Transistor Bias Voltages - Continued.

SUBASSEMBLY	TRANSISTOR	+VDC		
		E	B	C
Automatic Frequency Control A8	Q1	0.7	0.1	-7.2
	Q2	-7.9	-7.2	-7.9
	Q3	-7.9	-7.4	-7.9
	Q4	2.9	3.6	0.3
	Q5	0.0	0.3	5.2
	Q9	0.0	0.21	-0.64
	Q10	-0.64	0.0	-0.62
	Q11	-0.01	-1.2	14.0
	Q12	14.0	14.0	-0.65
	Q13	0.01	-0.65	0.0
	Q14	0.01	0.0	-7.3
	Q15	-7.9	-7.3	-7.9
Note: – Remove divider board A7A3 before measuring transistor bias voltage on display board A9A1.				
Display A9A1	Q1	0.0	+0.5	+0.5
	Q2	0.0	+0.5	+220.
	Q3	+219.5	+220.	+220.
	Q4	0.0	+0.5	+0.65
Gate Generator A9A2	Q1	8.1	8.7	15.0
	Q2	1.4	1.7	2.4
	Q3	0.0	-0.4	2.8
Divider A9A3	Q1	6.2	6.8	24.6
	Q2	0.0	0.6	5.0
First IF Amplifier A10	Q1	5.4	4.6	16.0
	Q3	4.9	5.4	20.5
	Q4	6.0	6.6	20.0
	Q5	22.5	23.0	25.0
	Q6	4.9	5.4	20.5
	Q7	6.0	6.6	20.0
	Q8	4.9	5.4	20.5
	Q9	6.0	6.6	20.0
Note: – Voltages at Q3 and Q4 measured with BAND-MHZ switch in position 2.7-5; Q6 and Q7 measured with BAND-MHZ switch in 1.5-2.7; Q8 and Q9 measured with BAND-MHZ switch in 9-17.				

Table 6-2 – Transistor Bias Voltages - Continued.

SUBASSEMBLY	TRANSISTOR	+VDC		
		E	B	C
Second Mixer A11	Q1	0.0	0.0	25.0
	Q2	25.0	25.0	0.0
	Q3	21.5	22.5	25.0
	Q4	0.0	0.0	25.0
	Q5	25.0	25.0	0.0
	Q6	-0.6	0.0	25.0
	Q7	-1.0	-0.5	24.5
	Q8	25.0	24.5	25.0
	Q9	17.5	24.0	-7.8
	Q10	-8.0	-7.8	-0.1
	Q11	0.0	3.8	0.0
	Q12	0.9	6.7	0.0
	Q13	3.0	11.5	0.0
	Q14	3.0	11.5	0.0
	Q15	7.5	16.0	0.0
	Q16	15.0	14.5	0.0
	Q19	15.0	14.5	0.0
	Q20	5.8	6.5	15.0
	Q21	5.8	6.5	21.0
Second IF Amplifier A12	Q1	6.8	7.4	20.5
	Q2	7.0	7.6	19.5
	Q3	6.8	7.4	24.0
	Q4	7.0	7.6	23.5
	Q5	24.5	23.5	12.0
	Q6	11.5	12.0	23.5
	Q7	5.8	6.4	25.0
	Q8	-0.6	0.0	16.0
Detector A13	Q1	-4.5	-4.0	0.0
	Q2	-5.1	-4.5	-0.58
	Q3	-0.58	0.01	24.2
	Q4	-0.58	0.0	20.0
	Q5	19.5	20.0	23.0
	Q6	5.5	6.1	16.0
	Q7	6.6	7.2	20.5
	Q9	6.6	7.2	20.5
	Q11	6.6	7.2	16.5
	Q12	16.0	16.5	23.5
	Q13	-0.55	0.0	23.5
	Q14	6.8	7.4	24.0
	Q15	6.8	7.4	21.5
	Q16	7.0	7.6	21.0
	Q17	7.0	7.6	24.0

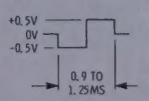
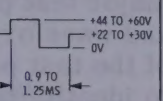
Table 6-2. – Transistor Bias Voltages – Continued.

SUBASSEMBLY	TRANSISTOR	+VDC		
		E	B	C
Detector A13 - Continued.	Q18	-0.87	-0.29	24.0
	Q19	7.2	7.8	24.0
	Q20	-4.6	-4.0	-0.22
	Q21	-0.22	0.02	24.0
	Q22	-0.22	0.0	16.5
	Q23	16.0	16.5	23.5
Independent Sideband A14	Q1	-4.6	-4.0	0.0
	Q2	-5.2	-4.6	-0.26
	Q3	-0.26	-0.01	25.0
	Q4	-0.26	0.0	19.0
	Q5	18.5	19.0	24.8
	Q6	0.0	0.6	12.0
	Q7	0.01	12.0	12.5
	Q8	0.0	12.5	0.01
	Q9	12.5	13.0	24.0
	Q10	24.8	24.0	12.5
	Q11	0.0	0.6	9.6
	Q12	9.1	9.6	25.0
	Q13	6.4	7.0	11.5
	Q14	6.5	7.1	17.5
	Q15	6.5	7.1	17.5
	Q16	17.8	17.5	0.0
	Q17	17.8	7.1	17.5
	Q18	2.9	3.4	24.5
Note: – Voltages at Q1 through Q5 measured with DETECTOR switch in LSB. Voltages at Q6 through Q12 measured with DETECTOR switch in ISB 6 KHZ.				
AF Amplifier A15	Q1	-0.7	-0.1	14.2
	Q2	0.0	0.6	10.0
	Q3	9.5	10.0	25.0
	Q4	0.0	0.6	9.4
	Q5	8.8	9.4	25.0
	Q6	0.0	0.5	11.0
	Q7	11.5	11.0	0.3
	Q8	0.0	0.3	11.5
	Q9	11.5	12.0	24.0
	Q10	24.5	24.0	11.5
	Q11	0.0	0.6	12.5
	Q12	13.0	12.5	0.1
	Q13	0.0	0.1	13.0
	Q14	13.0	13.5	24.5
	Q15	24.9	24.5	13.0

Table 6-2. – Transistor Bias Voltages – Continued.

SUBASSEMBLY	TRANSISTOR	+VDC		
		E	B	C
Beat Frequency Oscillator A22	Q1	4.5	5.0	10.2
	Q2	10.2	10.7	10.2
	Q3	7.2	7.9	23.7
Power Supply PS1	A1Q1	26.5	27.0	37.0
	A1Q2	25.6	26.5	37.0
	A1Q3	25.0	25.0	27.5
	A1Q4	27.0	27.5	31.0
	A1Q5	5.5	6.0	25.0
	A1Q6	5.5	6.0	27.0
	A1Q7	0.5	1.5	12.5
	A1Q8	0.15	0.5	7.0
	A1Q9	0.0	0.0	1.5
	A1Q10	-0.5	0.0	22.0
	A1Q11	-0.5	0.0	1.5
	A2Q1	219.5	220.0	225.0
	A2Q2	220.5	222.0	320.0
	A2Q3	220.0	219.0	222.0
	A2Q4	5.6	6.0	18.5
	A2Q5	5.2	5.6	10.0
	A2Q6	5.0	5.0	6.0
	A2Q7	16.0	15.5	5.6
	A2Q8	4.5	5.0	6.0
	A2Q9	4.5	5.0	20.5
	A2Q10	219.5	220.0	222.0
Power Supply PS2 (Optional)	A1Q1	26.5	27.0	37.0
	A1Q2	25.6	26.5	37.0
	A1Q3	25.0	25.0	27.5
	A1Q4	27.0	27.5	31.0
	A1Q5	5.5	6.0	25.0
	A1Q6	5.5	6.0	27.0
	A1Q7	0.5	1.5	12.5
	A1Q8	0.15	0.5	7.0
	A1Q9	0.0	0.0	1.5
	A1Q10	-0.5	0.0	22.0
	A1Q11	-0.5	0.0	1.5
	A2Q1	219.5	220.0	225.0
	A2Q2	220.5	222.0	320.0
	A2Q3	220.0	219.0	222.0
	A2Q4	5.6	6.0	18.5
	A2Q5	5.2	5.6	10.0
	A2Q6	5.0	5.0	6.0
	A2Q7	16.0	15.5	5.6
	A2Q8	4.5	5.0	6.0

Table 6-2. – Transistor Bias Voltages - Continued.

SUBASSEMBLY	TRANSISTOR	+VDC		
		E	B	C
Power Supply PS2 - Continued.	A2Q9	4.5	5.0	20.5
	A2Q10	219.5	220.0	222.0
	A3Q1 and A3Q2	0.0		
First Mixer A6	Q1	4.8	24.5	0.0
	Q2	4.8	24.5	0.0
	Q3	4.8	24.5	0.0
	Q4	4.8	24.5	0.0
First Local Oscillator A7A1	Q5	4.0	18.0	0.0
	Q6	4.0	18.0	0.0
	Q7	4.0	18.0	0.0
	Q8	4.0	18.0	0.0
	Q9	4.0	18.0	0.0
Automatic Frequency Control A8	Q6	5.2	6.2	7.9
	Q7	14.5	8.3	6.2
	Q8	17.0	6.2	7.9
First IF Amplifier A10	Q2	0.86	17.5	0.0
Second Mixer A11	Q17	6.5	21.5	0.0
	Q18	6.3	21.5	0.0
Detector	Q8	2.7	23.0	0.0
	Q10	2.3	23.0	0.0

6-4. PERFORMANCE TESTING. - The performance test procedures in this chapter are more detailed than those provided in Chapter 5 for preventive maintenance, and are designed to ensure proper performance of a receiver after repair and to assist in locating a malfunction when troubleshooting the receiver. When a component has been replaced or a subassembly has been repaired, the appropriate performance tests, and alignment procedures should be accomplished to ensure proper performance.

a. Nominal Test Point Voltages and Waveforms. - Table 6-3 lists all of the major test points provided in the receiver in numerical order. The expected voltages and waveforms for a normal operating receiver with known inputs are listed for each of the test points. Figures 6-1 through 6-5 provide different views of the receiver, to identify the location of all test points and controls. Refer to figure 2-4 in Chapter 2 for a rear view of the receiver identifying additional receiver test points. Figure 6-6 provides a test setup diagram showing basic equipment interconnected for the test results detailed in table 6-3. When checking voltages and waveforms as detailed in table 6-3, set the receiver controls as follows, unless otherwise specified.

LOCK-UNLOCK switch:	UNLOCK
BAND-MHZ switch:	as required
TUNE control:	tune to signal generator frequency
FINE TUNE control:	0, mid-position
RF GAIN control:	MAX
AUDIO GAIN control:	MAX
DETECTOR switch:	AM
IF BANDWIDTH switch:	16 kHz
FUNCTION switch:	MGC
ANTENNA TRIM control:	OFF
DIV TUNE-ANT DSBL switch:	OFF
NAR-WIDE Switch:	NAR
BFO kHz control:	0, mid-position
CARRIER-OFF-LINE switch:	OFF
ISB MONITOR switch:	CH A
LINE GAIN controls:	MAX

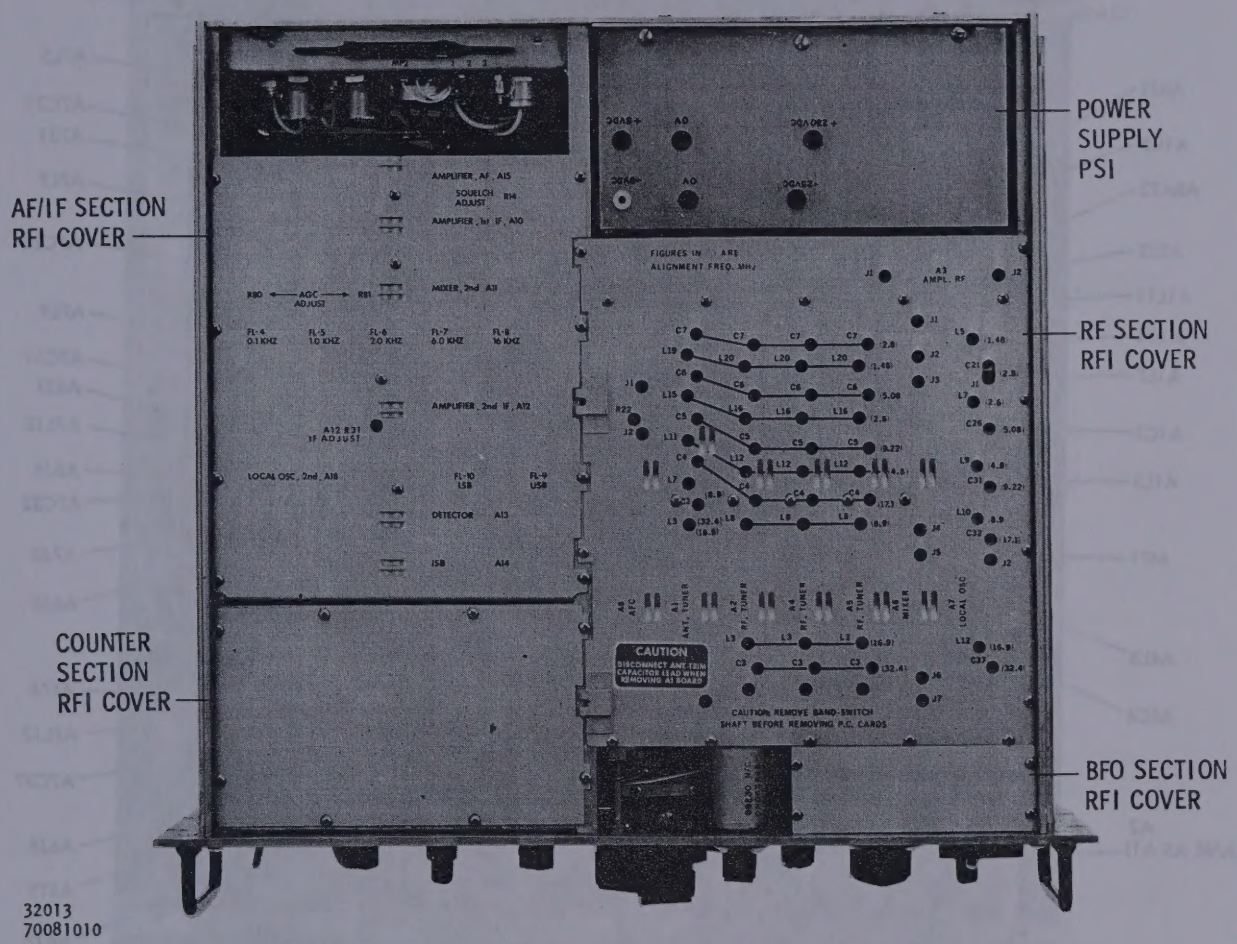


Figure 6-1. – Receiver Top View, RFI Covers Installed.

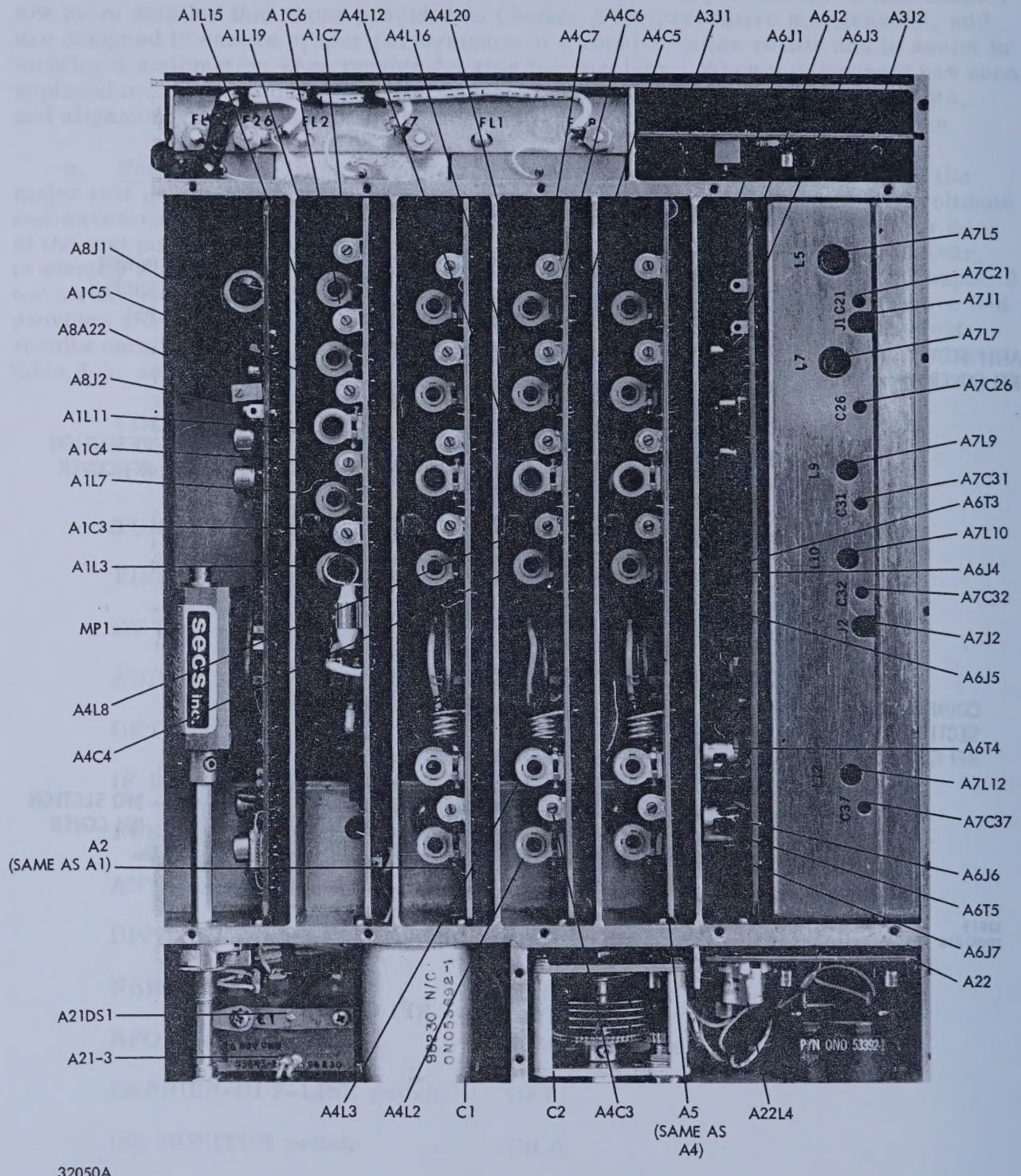


Figure 6-2. – RF Section, Identification of Controls and Test Points.

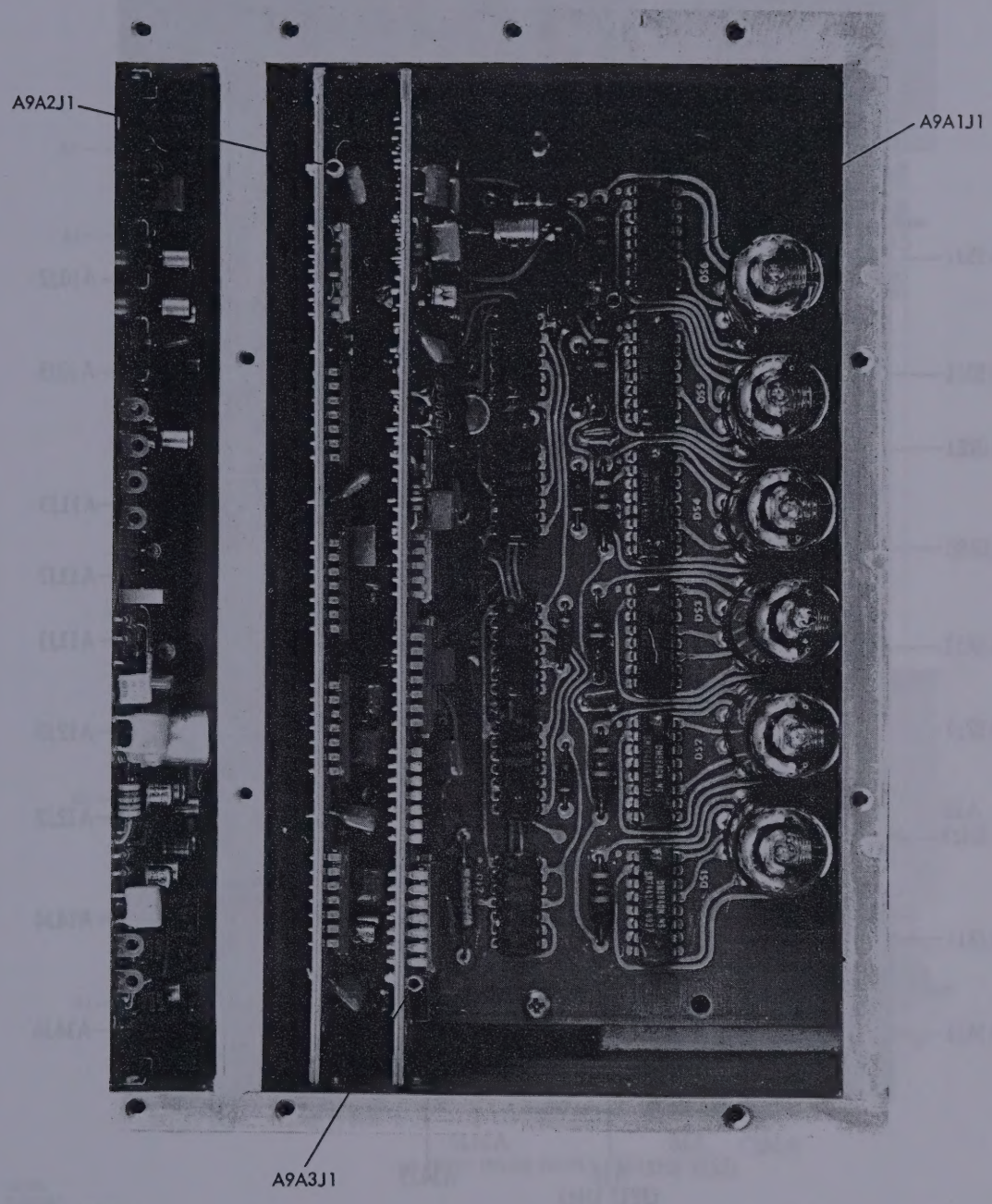


Figure 6-3. – Counter Section, Identification of Test Points.

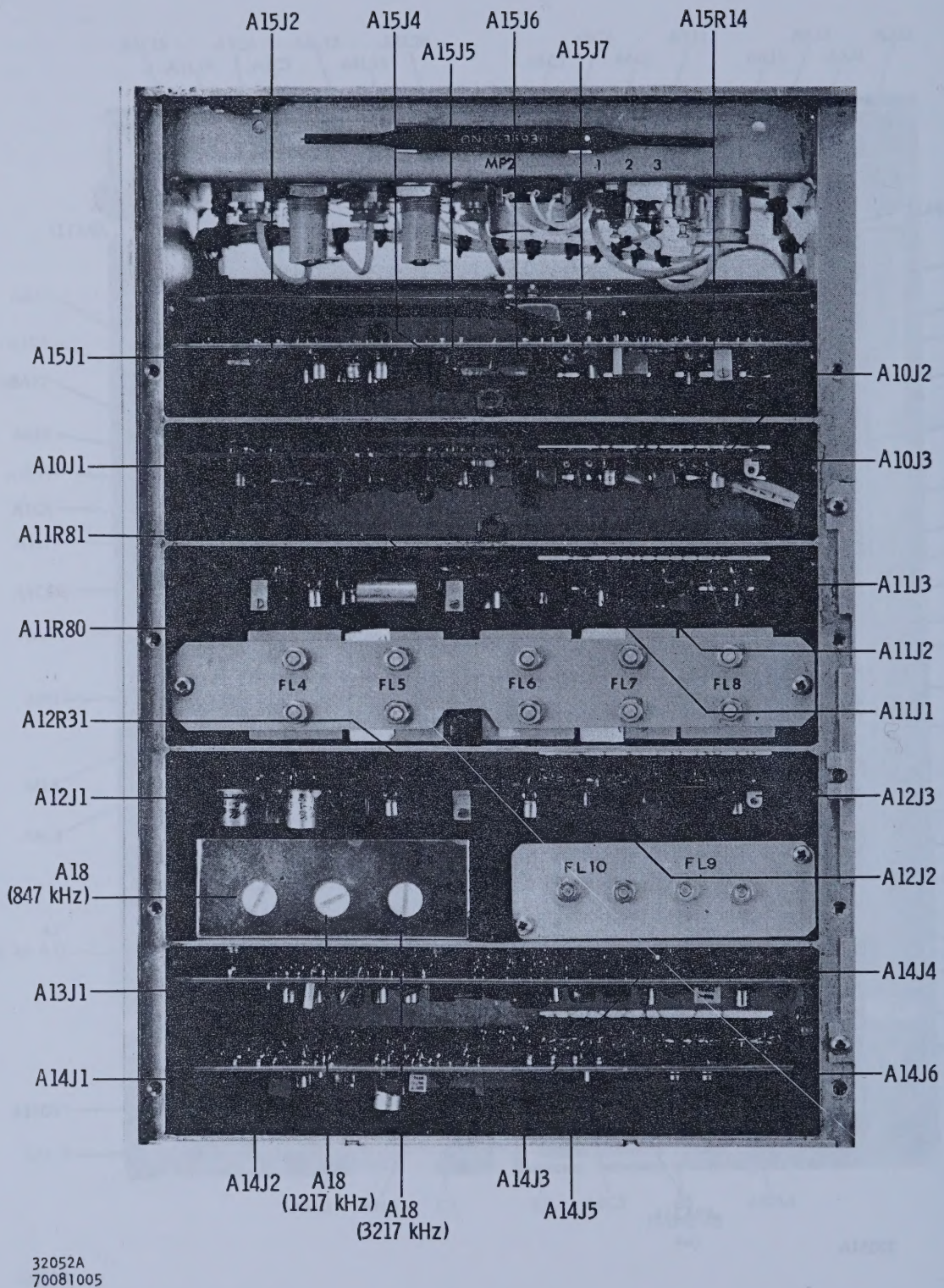
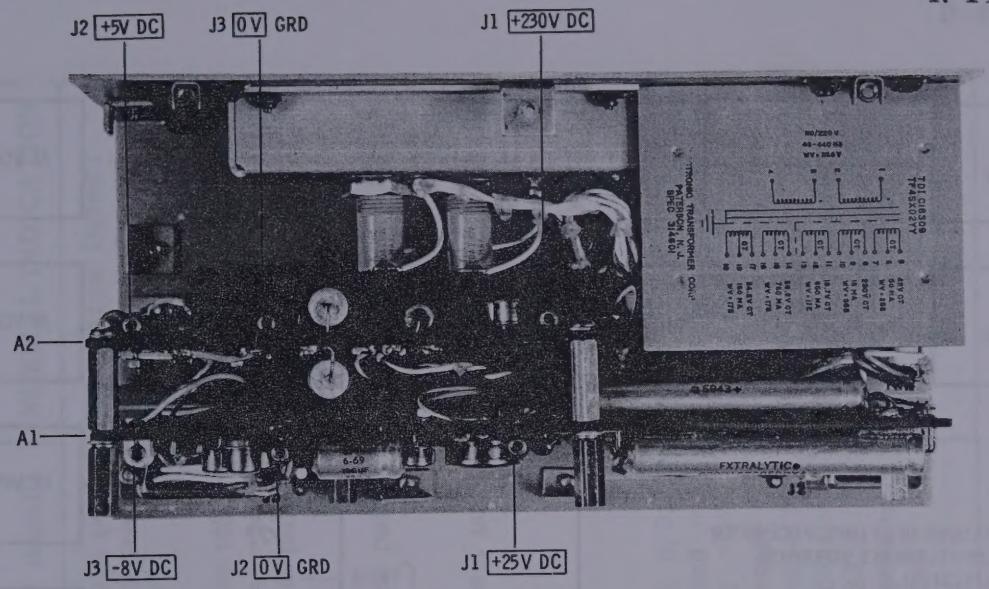
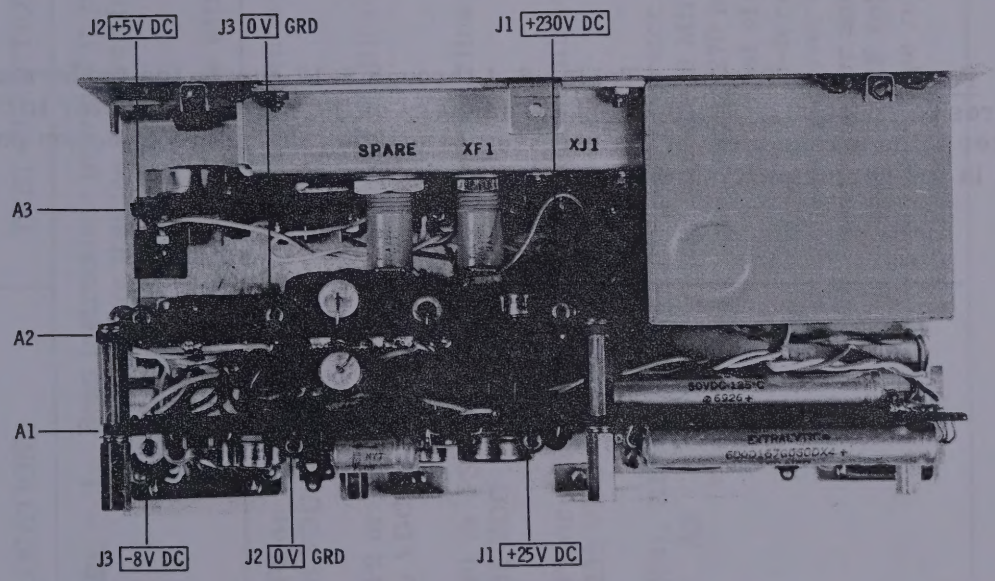


Figure 6-4. – AF/IF Section, Identification of Controls and Test Points.



AC INPUT POWER SUPPLY PS1



DC INPUT POWER SUPPLY PS2

32066
70081007
70081002

Figure 6-5. – Power Supplies, PS1 and PS2, Idenfitication of Test Points.

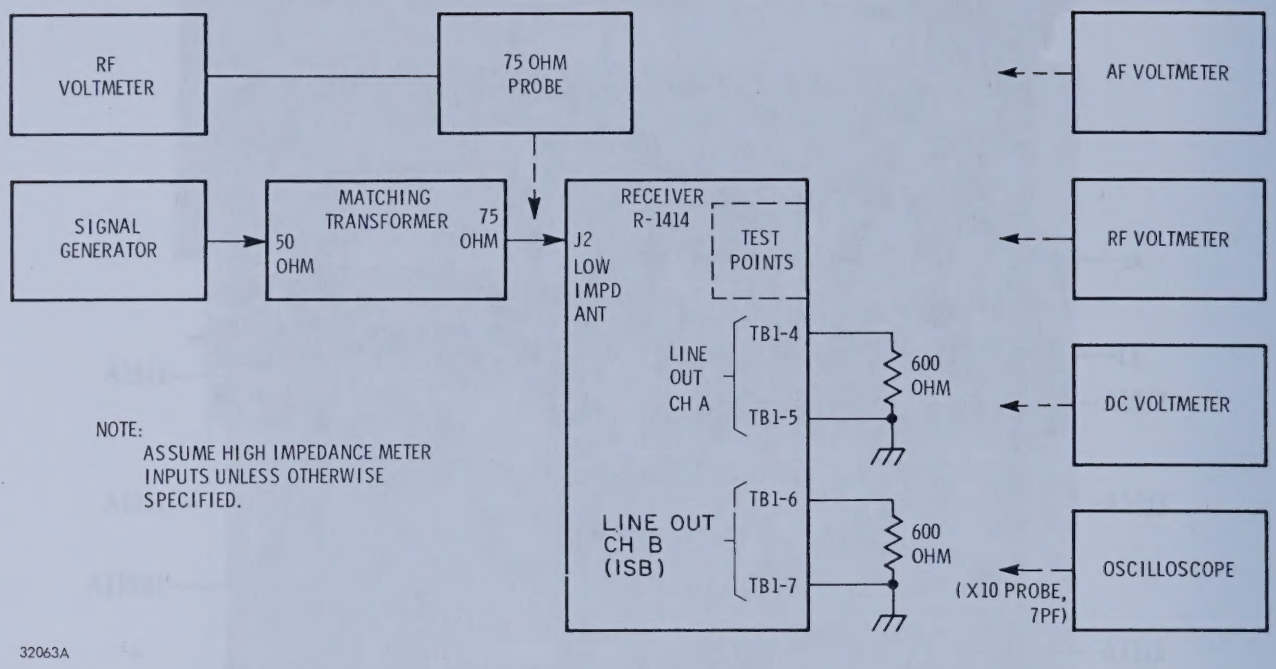


Figure 6-6. – Basic Test Setup Diagram.

b. Performance Tests. - Tables 6-4 through 6-17 supply the performance test procedures for checking the required parameters of the receiver. Refer to figure 2-4 in Chapter 2 for a rear view of the receiver identifying the interconnection points detailed in the performance tests.

Table 6-3. – Normal Test Point Outputs.

TEST POINT	LOCATION	TEST CONDITIONS (OTHER THAN BASIC)	NORMAL INDICATION
	Notes: – 1. Read instructions provided in paragraph 6-4 before performing any test listed below. Ensure that the receiver front panel controls are conditioned properly before continuing. 2. Use high impledance probe with voltmeters unless otherwise specified.		
1	PS1A1TP3 or PS2A1TP3 (WHT) -8 VDC output	Connect oscilloscope to -8 VDC test point.	-8(±0.2) volts, 1 mv max. pp ripple.
2	PS1A2TP2 or PS2A2TP2 (RED) +5 VDC output	Connect oscilloscope to +5 VDC test point.	+5 (±0.2) volts, 50 mv max. pp ripple.
3	PS1A1TP1 or PS2A1TP1 (RED) +25 VDC	Connect oscilloscope to +25 VDC test point.	+25(±0.4) volts, 1 mv max. pp ripple.
4	PS1A2TP1 or PS2A2TP1 (RED) +230 VDC	Connect oscilloscope to +230 VDC	+230(±15) volts, 5 volts max. pp ripple
5	A3J2 (GRN), RF input to RF ampl. A3	Signal generator set to 20.0, 10.0, 5.0, 3.0, and 2.0 MHz, unmodulated, and adjusted to 270 mv as measured at 75 ohm output of matching transformer with 75-ohm-terminated into RF voltmeter (receiver disconnected); reconnect receiver and measure TP5(A3J2) level with RF voltmeter (high impedance probe). Tune receiver for maximum indication.	80 mv to 240 mv

Table 6-3. – Normal Test Point Outputs - Continued.

TEST POINT	LOCATION	TEST CONDITIONS (OTHER THAN BASIC)	NORMAL INDICATION
6	A3J1 (GRN), RF output of RF ampl. A3	Signal generator set to 2.0 MHz, unmodulated, and level adjusted to 90 mv as measured at TP5 (A3J2), measure TP6 (A3J1) with RF voltmeter. Tune receiver for maximum indication at both test points.	360 mv to 540 mv
7	A6J4 (GRN) RF input to first mixer A6	Signal generator set to 2.0 MHz, unmodulated, and level adjusted to 1.0 V as measured at TP6 (A3J1); measure TP7 (A6J4) with RF voltmeter. Tune receiver for maximum indication at both test points.	630 mv to 1.1 volts
8	A6J5 (GRN), 0.392 MHz output of first mixer A6	Signal generator set to 2.0 MHz, unmodulated, and level adjusted to 300 mv as measured at TP7 (A6J4); measure TP8(A6J5) with RF voltmeter. Tune receiver for maximum indication at both test points.	500 mv to 3.0 volts
9	A6J6 (GRN), 0.762 MHz output of first mixer A6	Same as TP8 (A6J5) except signal generator set to 3.0 MHz; tune receiver to 3.0 MHz; BAND-MHZ switch to 2.7-5. Measure TP9(A6J6) with RF voltmeter. Tune receiver for maximum indication at both test points.	500 mv to 3.0 volts

Table 6-3. – Normal Test Point Outputs - Continued.

TEST POINT	LOCATION	TEST CONDITIONS (OTHER THAN BASIC)	NORMAL INDICATION
10	A6J7 (GRN), 2.762 MHz output of first mixer A6	Same as TP8 (A6J5), except signal generator set to 10.0 MHz; tune receiver to 10.0 MHz; BAND-MHZ switch to 9-17. Measure TP10 (A6J7) with RF voltmeter. Tune receiver for maximum indication at both test points.	500 mv to 3.0 volts
11	A6J3 (YEL), output of LO	Tune receiver to 2.0, 3.0, 5.0, 10.0, and 20.0 MHz (signal generator not used); measure TP11 (A6J3) with RF voltmeter.	1.5 volts to 2.5 volts
12	A6J2 (YEL), Intermediate output of LO amplifier on first mixer A6	Same as for TP11 (A6J3)	100 mv to 320 mv
13	J4 (rear panel) LOC OSC IN/OUT, first LO output or external LO input	Same as for TP11 (A6J3) except measure with RF voltmeter using 50-ohm probe.	400 mv to 1.1 volts
14	A10J2 (GRN), 0.392, 0.762, and 2.762 MHz input to first IF ampl. A10	Signal generator set to 2.0 MHz, unmodulated, and level adjusted to 0.5 volt as measured at TP8 (A6J5); measure TP14 TP14 (A10J2) with RF voltmeter.	150 mv to 400 mv
		Signal generator set to 3.0 MHz, unmodulated, and level adjusted to 0.5 volts as measured at TP9 (A6J6); measure TP14(A10J2) with RF voltmeter.	150 mv to 400 mv

Table 6-3. – Normal Test Point Outputs - Continued.

TEST POINT	LOCATION	TEST CONDITIONS (OTHER THAN BASIC)	NORMAL INDICATION
15	A10J3 (YEL), AGC No. 2 input to first IF ampl. A10	Tune receiver to 10.0 MHz (signal generator not used); measure TP15 (A10J3) with DC voltmeter.	0.0 vdc to +0.2 vdc
16 and 17	A10J1 (GRN), IF output of first IF ampl. A10 A11J1 (GRN), IF input to second mixer A11	Signal generator set to 2.0 MHz, unmodulated, and level adjusted to 12 mv as measured at TP 14 (A10J2); measure TP 16 (A10J1) and TP 17 (A11J2) with RF voltmeter.	100 to 500 mv
		Signal generator set to 3.0 MHz, unmodulated, and level adjusted to 12 mv as measured at TP14 (A10J2); measure TP16 (A10J1) and TP17 (A11J2) with RF voltmeter.	100 to 500 mv
		Signal generator set to 10.0 MHz, unmodulated, and level adjusted to 12 mv as measured at TP14 (A10J2); measure TP16 (A10J1) and TP17 (A11J2) with RF voltmeter.	100 to 500 mv
18	A11J2 (GRN), LO input to second mixer A11	Tune receiver to 2.0, 3.0, and 10.0 MHz (signal generator not used); measure TP18 (A11J2) with RF voltmeter.	800 mv to 1.5 volts
19	A11J3 (GRN), IF output of second mixer A11	Signal generator set to 2.0, 3.0 and 10.0 MHz, unmodulated, and level adjusted to 250 mv as measured at TP17 (A11J1); measure TP19 (A11J3) with RF voltmeter.	150 mv to 700 mv

Table 6-3. – Normal Test Point Outputs - Continued.

TEST POINT	LOCATION	TEST CONDITIONS (OTHER THAN BASIC)	NORMAL INDICATION
20	J5 (rear panel) SDU OUT, IF output of second mixer A11 for display purposes	Same as above, except measure TP20 (J5) with RF voltmeter and 50-ohm probe.	15 mv to 70 mv
21	A12J3 (YEL), IF input to second IF amplifier A12	Signal generator set to 2.0 MHz, unmodulated, and level set to 300 mv as measured at TP19 (A11J3); measure TP21 (A12J3) with RF voltmeter.	60 mv to 230 mv
22	A12J2 (GRN), AGC No. 3 input to second IF amplifier A12	Tune receiver to 2.0 MHz (signal generator not used); measure TP22 (A12J2) with dc voltmeter.	0.0 vdc to 0.3 vdc
23	J6 (rear panel) IF OUT, IF output from second IF amplifier A12 at rear panel	Signal generator set to 32.0 MHz, unmodulated, -99 dbm; measure TP23 (J6) with RF voltmeter using 50 ohm termination.	20 mv to 100 mv
24	A12J1 (GRN), IF output of second IF amplifier A12	Same as TP23 (J6) except measure TP24 (A12J1) with RF voltmeter and high impedance probe.	100 mv to 450 mv
25	A7J2, +25 V voltage regulator output on first LO A7	Measure TP25 (A7J2) with dc voltmeter.	22 vdc to 25 vdc
26	A7J1, LO output to counter on first LO A7	Tune receiver to 2.0 MHz. Measure TP26 (A7J1) with RF voltmeter.	30 mv to 70 mv
27	A8J1 (GRN), AFC voltage output from AGC A8	Tune receiver to 2.0 MHz (signal generator not used); measure TP27 (A8J1) with dc voltmeter.	+6 vdc to +9 vdc

Table 6-3. – Normal Test Point Outputs - Continued.

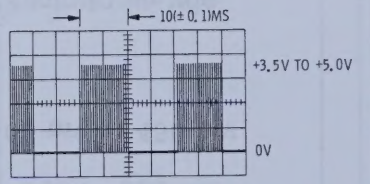
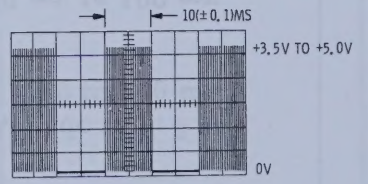
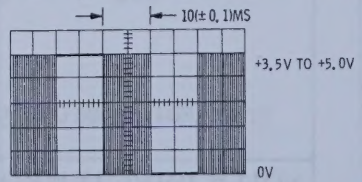
TEST POINT	LOCATION	TEST CONDITIONS (OTHER THAN BASIC)	NORMAL INDICATION
28	A8J2 (YEL), Integration pulse width output of variable pulse width network on AFC A8	Measure TP28 (A9J2) with dc voltmeter.	-5 vdc to -9 vdc
29	A9A1J1 (GRN), Divided-by-10 LO input to display A9A1	Measure TP29 (A9A1J1) with oscilloscope. Vert. defl. set for 1.0 V/cm and horiz. time base set for 5 ms/cm	
30	A9A3J1 (GRN), Sum output of divider A9A3	Same as TP29 (A9A1J1), except measure at TP30 (A9A3J1).	 (A9A3J1) SUM OUTPUT OF DIVIDER A9A3, RECEIVER NOT BEING TUNED, AFC WORKING (NORMAL DISPLAY)  (A9A3J1) SUM OUTPUT OF DIVIDER A9A3, RECEIVER TUNING JUST STOPPED, AFC WORKING (TEMPORARY DISPLAY)

Table 6-3. – Normal Test Point Outputs - Continued.

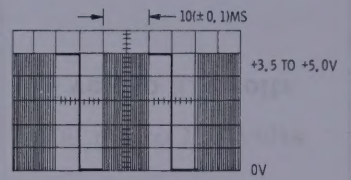
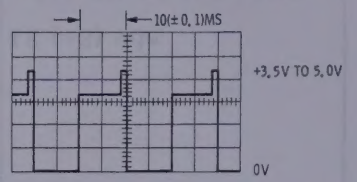
TEST POINT	LOCATION	TEST CONDITIONS (OTHER THAN BASIC)	NORMAL INDICATION
30 Cont.			 (A9A3J1) SUM OUTPUT OF DIVIDER A9A3, RECEIVER BEING TUNED, AFC DISABLED
31	A9A2J1 (YEL), Basic 50 kHz gating rate output of gate generator A9A2.	Same as TP29 (A9A1J1), except measure at TP31 (A9A2J1)	 (A9A2J1) BASIC 50 kHz GATING RATE
32	A13J1 (GRN), AGC output of detector A13	Signal generator set to 2.0 MHz, unmodulated. Set FUNCTION switch to AGC-S, measure TP32 (A13J1) with DC voltmeter while varying the signal. generator output from -110 dbm to 0 dbm.	-10 vdc to +10 vdc

Table 6-3. – Normal Test Point Outputs - Continued.

TEST POINT	LOCATION	TEST CONDITIONS (OTHER THAN BASIC)	NORMAL INDICATION
33	A14J1 (GRN), IF input to ISB A14	Set FUNCTION switch to MGC. Set signal generator to 2.0 MHz, unmodulated -99 dbm; measure TP33 (A14J1) with RF voltmeter. Tune receiver for maximum output.	Greater than 90 mv
34	A14J6 (GRN), LSB filter IF input to ISB A14	Same as TP33 (A14J1), except measure with RF voltmeter at TP34 (A14J6).	Greater than 40 mv
35	A14J4 (GRN), BFO A22 Crystal oscillator input to LSB product detector in ISB A14.	Set DETECTOR switch to LSB, USB, or ISB; measure TP35 (A14J4) with RF voltmeter.	150 mv to 350 mv
36	A14J5 (GRN), LSB product detector output of ISB A14	a. Set DETECTOR switch to ISB 6 KHZ. Measure TP36 (A14J5) with dc voltmeter.	18 (±3) vdc
		b. Set signal generator to 2.0 MHz, unmodulated, -99 dbm, and tune signal generator frequency for maximum AF output at TP36 (A14J5); measure with ac voltmeter.	0.5 volt to 3.0 volts
37	A14J3 (GRN), Channel B ISB output of ISB A14	Same as for TP36b (A14J5), except measure TP37 (A14J3) with ac voltmeter.	0.8 volt to 3.0 volts
38	A14J2 (GRN), Line gain audio output of ISB A14	Same as for TP36b (A14J5), except measure TP38 (A14J2) with ac voltmeter.	More than 1.5 volts.

Table 6-3. – Normal Test Point Outputs - Continued.

TEST POINT	LOCATION	TEST CONDITIONS (OTHER THAN BASIC)	NORMAL INDICATION
39	TB1-6, -7 LINE OUT CH B (ISB) (rear panel), ISB line audio output at rear panel	Same as TP38 (A14J2); measure between TB1-6 and TB1-7 with ac voltmeter.	More than 0.775 volt
40	A14J7 (GRN), Audio input to AF Amplifier A15	Set signal generator to 2 MHz modulated, 400 Hz, 30 percent. Set DETECTOR switch to AM. Adjust signal generator for 350 mv at TP24 (A12J1). Measure TP40 (A14J7) with ac voltmeter.	500 mv to 1.8 volts
		Set signal generator to 2 MHz, unmodulated. Set DETECTOR switch to CW. Set BFO KHZ control to +1. Adjust signal generator to 350 mv at TP24 (A12J1). Measure TP40 (A15J7) with ac voltmeter.	400 mv to 1.8 volts
		Set signal generator to 2 MHz, unmodulated with level set for 350 mv at TP24 (A12J1). Set DETECTOR switch to USB. Measure TP40 (A14J7) with ac voltmeter.	500 mv to 3.0 volts
		Condition FM signal generator for 5.6 kHz deviation at 400 Hz modulation. Set DETECTOR switch to FM. Set level for 350 mv at TP24 (A12J1). Measure TP40 (A14J7) with ac voltmeter.	150 mv to 600 mv

Table 6-3. – Normal Test Point Outputs - Continued.

TEST POINT	LOCATION	TEST CONDITIONS (OTHER THAN BASIC)	NORMAL INDICATION
41	A15J5 (GRN), Channel A audio input to line audio ampl in AF ampl. A15	Set DETECTOR switch to ISB 6 KHZ. Signal generator to approximately 2.0 MHz, unmodulated, -99 dbm. Tune receiver for maximum output on ac voltmeter connected to TP41 (A14J5).	0.5 volt to 4.0 volts
42	A14J2 (GRN), Line audio output of AF Amplifier A15 to rear panel and to carrier-line meter M1.	Set DETECTOR switch to ISB 6 KHZ. Set signal generator to 2.0 MHz, unmodulated, -99 dbm, and tune the signal generator frequency for maximum audio output at TP42 (A15J2),	More than 1.5 volts
43	TB1-4, -5 LINE OUT CH A (rear panel), Line audio output of AF amplifier A14 at rear panel	Same as TP42 (A14J2); measure TB1-4 and TB1-5 with ac voltmeter.	More than 1 volt
44	A15J6 (GRN), Audio output from NAR position of NAR-WIDE switch to audio filter on AF amplifier A15	Same as TP42 (A15J2), except set ISB MONITOR switch to CH B. Set audio NAR-WIDE switch to NAR. Measure TP44 (A15J6) with ac voltmeter.	More than 0.5 volt
45	A15J4 (GRN), audio output from NAR-WIDE switch to audio ampl on AF ampl A15	Same as TP44 (A15J6), except audio NAR-WIDE switch may be in either NAR or WIDE position. Measure TP45 (A15J4) with ac voltmeter.	More than 0.5 volt

Table 6-3. – Normal Test Point Outputs - Continued.

TEST POINT	LOCATION	TEST CONDITIONS (OTHER THAN BASIC)	NORMAL INDICATION
46	A15J1 (GRN), phone audio output of AF amplifier A15 to PHONES jack on front panel and PHONE AUDIO OUT on rear panel	Same as TP45 (A15J4), except measure TP46 (A15J1) with ac voltmeter.	More than 5.5 volts
47	J7 PHONES (front panel). Audio output of AF amplifier A15 at PHONES jack on front panel.	Same as TP45 (A15J4), except measure TP47 (J7) with ac voltmeter.	More than 5.5 volts
48	TB1-8, PHONE AUDIO OUT (rear panel), Phone audio output of AF amplifier A15 at rear panel.	Same as TP45 (A15J4), except measure TP48 (TB1-8) with ac voltmeter.	More than 5.5 volts

Table 6-4. – Noise Figure (Noise Generator Method), Performance Test

STEP	PROCEDURE	NORMAL INDICATION
1	Connect equipment as shown in figure 6-7. Do not turn-on equipment.	
2	Adjust receiver controls and switches as follows: FUNCTION switch: MGC ANTENNA TRIM control: OFF DIV TUNE-ANT DSBL switch: OFF RF GAIN control: MAX DETECTOR switch: AM FINE TUNE control: 0, mid-position LOCK-UNLOCK switch: UNLOCK IF BANDWIDTH switch: 6 kHz	
3	Adjust noise generator current adjustment to lowest level.	
4	Adjust attenuator to 0 db.	
5	Turn-on receiver and RF voltmeter. (Leave noise generator turned-off.)	
6	Tune receiver as follows: TUNE control: 1.5 MHZ BAND-MHZ switch: 1.5-2.7 MHZ	
7	Record IF output voltage on RF voltmeter.	
8	Adjust attenuator to 3 db of attenuation.	
9	Turn-on noise generator.	
10	Increase noise generator current until same IF output level, as in step 7, is again obtained.	
11	Read noise figure directly from face of noise generator meter.	Must not exceed 10 db.
12	Turn-off noise generator.	
13	Adjust noise generator current adjustment to lowest level.	

Table 6-4. – Noise Figure (Noise Generator Method), Performance Test - Continued.

STEP	PROCEDURE		NORMAL INDICATION
14	Adjust attenuator to 0 db.		
15	Repeat steps 7 through 14 for each of the following adjustments of receiver tune control and BAND-MHZ switch:		Same as for steps 7 through 11.
	BAND MHZ	TUNE	
	1.5-2.7	2.0	
	1.5-2.7	2.7	
	2.7-5	2.7	
	2.7-5	4.0	
	2.7-5	5.0	
	5-9	5.0	
	5-9	7.0	
	5-9	9.0	
	9-17	9.0	
	9-17	12.0	
	9-17	17.0	
	17-32	17.0	
	17-32	24.0	
	17-32	32.0	

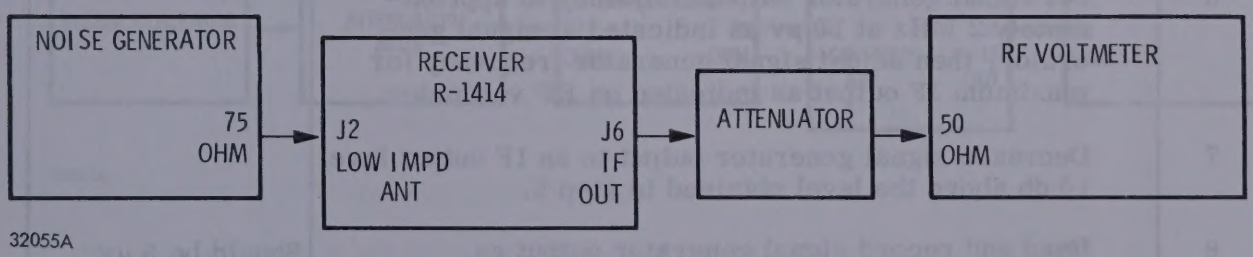


Figure 6-7. – Noise Figure Test Setup Diagram.

Table 6-5. – Sensitivity Check (Alternate for Noise Figure), Performance Test.

STEP	PROCEDURE	NORMAL INDICATION
1	Connect equipment as shown in figure 6-8.	
2	Turn-on receiver and RF voltmeter.	
3	Adjust receiver controls as follows: BAND-MHZ switch: 1.5-2.7 LOCK-UNLOCK UNLOCK TUNE control: 2.0 MHz FUNCTION switch: MGC NAR-WIDE switch: WIDE ANTENNA TRIM control: OFF DIV TUNE-ANT DSBL switch: OFF RF GAIN control: MAX FINE TUNE control: 0, mid-position BFO KHZ control: 0, mid-position DETECTOR switch: AM IF BANDWIDTH switch: 6 kHz NOISE LIMITER control: OFF LINE GAIN control: MAX AUDIO GAIN control: MAX	
4	Tune receiver to 2 MHz and set signal generator power output to minimum.	
5	Read and record IF noise output as indicated on RF voltmeter.	
6	Set signal generator output frequency to approximately 2 MHz at 10 μv as indicated at signal generator, then adjust signal generator frequency for maximum IF output as indicated on RF voltmeter.	
7	Decrease signal generator output to an IF output level 10 db above the level obtained in step 5.	
8	Read and record signal generator output as indicated at signal generator.	Should be 5 μv or less
9	Repeat steps 4 through 8 for the following BAND-MHZ switch and TUNE control settings (and signal generator frequencies):	Same as for step 8

Table 6-5. – Sensitivity Check (Alternate for Noise Figure), Performance Test. - Continued.

STEP	PROCEDURE		NORMAL INDICATION
9 Cont.	BAND-MHZ switch	TUNE control (MHz)	
	1.5-2.7	2.0	
	1.5-2.7	2.7	
	2.7-5	2.7	
	2.7-5	4.0	
	2.7-5	5.0	
	5-9	5.0	
	5-9	7.0	
	5-9	9.0	
	9-17	9.0	
	9-17	12.0	
	9-17	17.0	
	17-32	17.0	
	17-32	24.0	
	17-32	32.0	

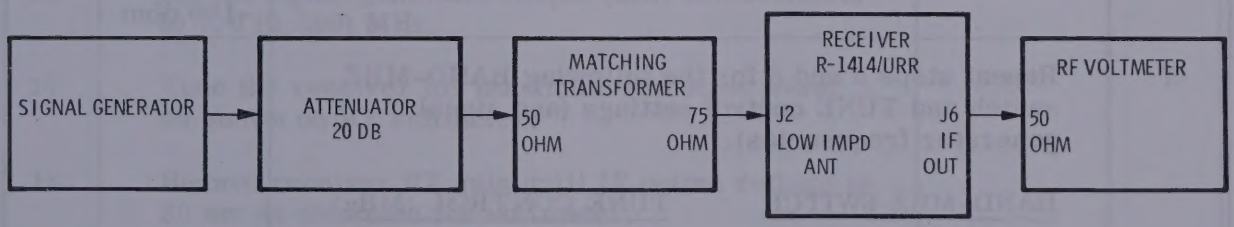


Figure 6-8. – Sensitivity Check, Test Setup Diagram

Table 6-6. – Overall Gain, Audio Power, IF Output, Performance Tests.

STEP	PROCEDURE	NORMAL INDICATION
1	Connect the equipment as shown in figure 6-9.	
2	Turn-on receiver and test equipment.	
3	Adjust receiver controls and switches as follows: BAND-MHZ switch: 1.5-2.7 MHz LOCK-UNLOCK control: UNLOCK TUNE control: 1.5 MHz (approx) FUNCTION switch: MGC ANTENNA TRIM control: OFF DIV TUNE-ANT DSBL switch: OFF AUDIO GAIN control: MAX RF GAIN control: MAX DETECTOR switch: AM IF BANDWIDTH switch: 6 kHz NOISE LIMITER control: OFF LINE GAIN control: MAX	
4	Tune the signal generator to 1.5 MHz cw.	
5	Adjust the signal generator output level for a detector output voltage of 2(±0.05) volts as indicated on the DC voltmeter.	
6	Record the signal generator output level (in dbm).	Approximately -100 dbm
7	Repeat steps 5 and 6 for the following BAND-MHZ switch and TUNE control settings (and signal generator frequencies). BAND-MHZ SWITCH — TUNE CONTROL (MHz) 1.5-2.7 — 2.0 1.5-2.7 — 2.7 2.7-5 — 2.7 2.7-5 — 4.0 2.7-5 — 5.0 5-9 — 5.0 5-9 — 7.0 5-9 — 9.0 9-17 — 9.0 9-17 — 12.0 9-17 — 17.0 17-32 — 17.0 17-32 — 24.0 17-32 — 32.0	

Table 6-6. – Overall Gain, Audio Power, IF Output, Performance Tests - Continued.

STEP	PROCEDURE	NORMAL INDICATION
8	Compare results of steps 6 and 7 for all 15 frequencies.	Variation in signal generator output levels should not exceed 10 dbm
9	Adjust signal generator to the test frequency that caused the highest signal generator input level.	
10	Set signal generator output to -99 dbm, with 30 percent modulation at 400 Hz.	
11	Tune the receiver for maximum IF response.	
12	Record the line audio power shown on AC voltmeter connected to LINE OUT CH A terminals (TB1-4 and TB1-5).	Should be equal to or greater than 0 dbm (0.775 volts)
13	Record the phone audio power shown on AC voltmeter connected to PHONE AUDIO OUT terminal TB1-8.	Should be equal to or greater than +17 dbm (5.5 v).
14	Turn the signal generator modulation off (cw mode).	
15	Record the IF output level shown in the RF voltmeter.	Should be greater -21 dbm (20 mv).
16	Set the signal generator output (still unmodulated) to 7.0 (0.500) MHz.	
17	Tune the receiver for maximum IF output power as shown on RF voltmeter.	
18	Reduce receiver RF gain until IF output voltage is 20 mv as shown on RF voltmeter.	
19	Increase signal generator output to -79 dbm.	
20	Record IF output voltage as shown on RF voltmeter.	200 (±20) mv
21	Set receiver AUDIO GAIN control to MAX.	
22	Set receiver LINE GAIN and RF GAIN controls to MAX.	
23	Set DETECTOR switch to LSB.	

Table 6-6. – Overall Gain, Audio Power, IF Output, Performance Tests - Continued.

STEP	PROCEDURE	NORMAL INDICATION
24	Tune the receiver to 7.0010 MHz.	
25	Set signal generator frequency to 7.0 MHz ±100 Hz and adjust its output level for 0 dbm on AC voltmeter connected to LINE OUT CH A terminals (TB1-4 and TB1-5).	
26	Record signal generator output level.	Should be less than -99 dbm
27	Adjust signal generator output level for +17 dbm indication on AC voltmeter connected to PHONE AUDIO OUT terminal TB1-8.	
28	Record signal generator output level.	Should be less than -99 dbm
29	Set DETECTOR switch to USB.	
30	Tune the receiver to 6.9990 MHz.	
31	Repeat steps 25 through 28.	Same as for steps 25 through 28.
32	Set DETECTOR switch to CW.	
33	Tune Receiver to 7.0000 MHz.	
34	Adjust RBO KHZ control to +1 kHz.	
35	Repeat steps 25 through 28.	Same as for steps 25 through 28.

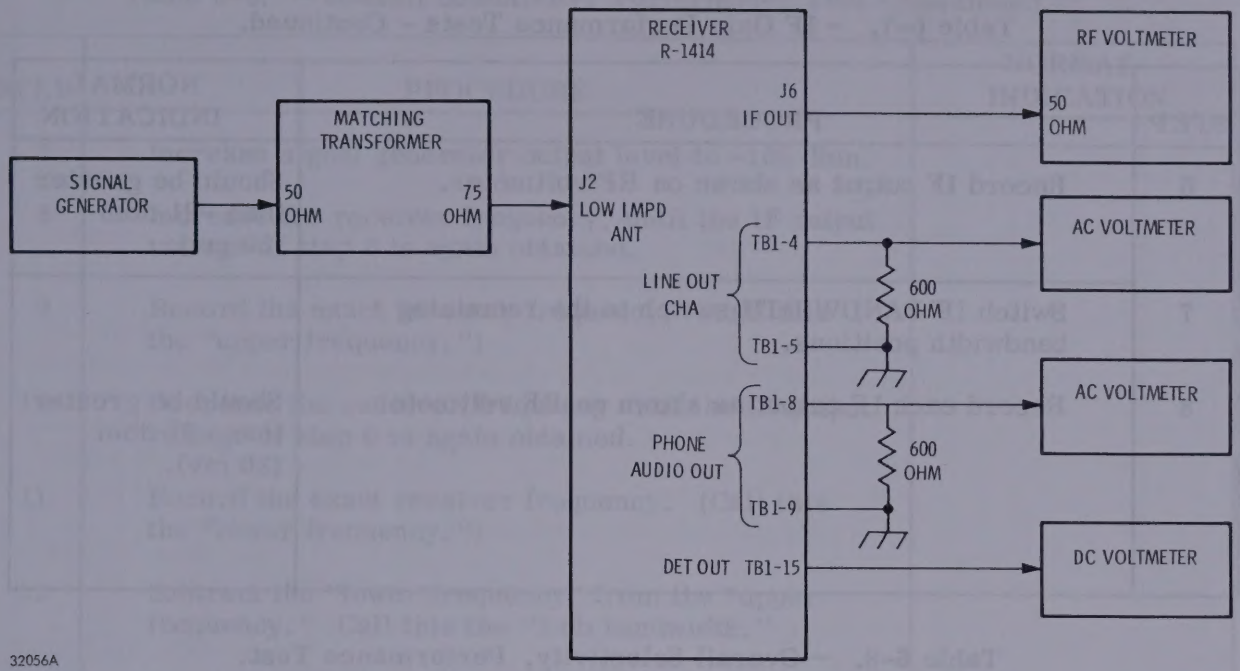


Figure 6-9. – Overall Gain, Test Setup Diagram.

Table 6-7. – IF Gain Performance Tests.

STEP	PROCEDURE	NORMAL INDICATION
1	Connect the equipment as shown in figure 6-8, except delete the attenuator.	
2	Turn-on receiver and test equipment.	
3	Adjust receiver control and switches as follows: TUNE control: To frequency established in table 6-6, step 9 BAND-MHZ switch: As required FUNCTION switch: MGC ANTENNA TRIM control: OFF DIV TUNE-ANT DSBL switch: OFF AUDIO GAIN control: MAX RF GAIN control: MAX FINE TUNE control: 0, mid-position LOCK-UNLOCK control: UNLOCK IF BANDWIDTH switch: 0.1 kHz	
4	Adjust signal generator to the test frequency established in table 6-6 (as indicated by receiver frequency display and maximum indication on RF voltmeter.	
5	Adjust signal generator output for -99 dbm cw signal.	

Table 6-7. – IF Gain Performance Tests - Continued.

STEP	PROCEDURE	NORMAL INDICATION
6	Record IF output as shown on RF voltmeter.	Should be greater than -21 dbm (20 mv).
7	Switch IF BANDWIDTH switch to the remaining bandwidth positions.	
8	Record each IF output as shown on RF voltmeter.	Should be greater than -21 dbm (20 mv).

Table 6-8. – Overall Selectivity, Performance Test.

STEP	PROCEDURE	NORMAL INDICATION
1	Connect the equipment as shown in figure 6-8 except for attenuator.	
2	Turn-on receiver and test equipment.	
3	Adjust the receiver controls and switches as follows: BAND-MHZ switch: 5-9 MHz TUNE control: 7.0 MHz FUNCTION switch: MGC ANTENNA TRIM control: OFF DIV TUN-ANT DSBL switch: OFF RF GAIN control: MAX FINE TUNE control: 0, mid position LOCK-UNLOCK: UNLOCK IF BANDWIDTH switch: 16 kHz NOISE LIMITER control: OFF	
4	Tune the signal generator to 7.0 MHz, and adjust the output level to -108 dbm, unmodulated (CW).	
5	Adjust the receiver frequency for maximum receiver IF output voltage, as indicated on the RF voltmeter.	
6	Record the IF output voltage and receiver frequency.	

Table 6-8. – Overall Selectivity, Performance Test - Continued.

STEP	PROCEDURE	NORMAL INDICATION
7	Increase signal generator output level to -105 dbm.	
8	Increase the receiver frequency, until the IF output voltage of step 6 is again obtained.	
9	Record the exact receiver frequency. (Call this the "upper frequency.")	
10	Decrease the receiver frequency until the IF output voltage of step 6 is again obtained.	
11	Record the exact receiver frequency. (Call this the "lower frequency.")	
12	Subtract the "lower frequency" from the "upper frequency." Call this the "3 db bandwidth."	
13	Increase the signal generator output level to -48 dbm.	
14	Repeat steps 8 through step 11.	
15	Subtract the "lower frequency" from the "upper frequency." Call this the "60 db bandwidth."	
16	Repeat steps 4 through step 15 for the following settings of the IF BANDWIDTH switch: 6 kHz 2 kHz 1 kHz 0.1 kHz (at discretion maintenance supervisor, accuracy limited to ±0.1 kHz)	
17	Compare results to required limits.	Required Limits IF BANDWIDTH switch / Minimum 3 db bandwidth / Maximum 60 db bandwidth 16 — 16 kHz — 32 kHz 6 — 6 kHz — 13 kHz 2 — 2 kHz — 5.5 kHz

Table 6-8. – Overall Selectivity, Performance Test - Continued.

STEP	PROCEDURE	NORMAL INDICATION
17 Cont.		IF BAND-WIDTH switch / Minimum 3 db bandwidth / Maximum 60 db bandwidth Note: – If the 2 kHz filter is replaced by an optional filter the normal indication would be as follows: 2 (FL21): 3.5 kHz / 8.75 kHz 2 (FL22): 3.0 kHz to 3.5 kHz / 15.0 kHz 1: 1 kHz / 3.3 kHz 0.1: 0.1 kHz / 1 kHz
18	Repeat steps 4 through 6 at 1.5 MHz and 32 MHz but use only the 6 kHz and 16 kHz filters.	

Table 6-9. – Antenna Grounding Relay Attenuation, Performance Test.

STEP	PROCEDURE	NORMAL INDICATION
1	Connect the equipment as shown in figure 6-8 except for attenuator.	
2	Connect a jumper wire between the ANTENNA DISABLE INPUT (TB1-1) and GRD (TB1-2).	
3	Turn-on receiver and test equipment.	
4	Adjust the receiver controls as follows: LOCK-UNLOCK control: UNLOCK BAND-MHZ switch: 17-32 MHz TUNE control: 30 MHz FUNCTION switch: MGC NAR-WIDE switch: WIDE RF GAIN control: MAX	

Table 6-9. – Antenna Grounding Relay Attenuation, Performance Test - Continued.

STEP	PROCEDURE	NORMAL INDICATION
4 Cont.	ANTENNA TRIM control: OFF DIV TUNE-ANT DSBL switch: OFF FINE TUNE control: 0, mid-position DETECTOR switch: AM IF BANDWIDTH switch: 16 kHz NOISE LIMITER control: OFF	
5	Tune the signal generator to the center of the receiver passband by tuning the signal generator for a maximum IF output as indicated on the RF voltmeter.	
6	Adjust the signal generator output for -88 dbm cw.	
7	Adjust the receiver RF GAIN control for 20.0 mv IF output voltage, measured with the RF voltmeter.	
8	Set DIV TUNE-ANT DSBL switch to ON.	
9	Increase the signal generator output level until the RF voltmeter shows the IF output to be 20 mv again.	
10	Read the signal generator output level.	Should be at least -28 dbm.
11	Switch DIV TUNE-ANT DSBL switch to OFF.	
12	Connect equipment as shown in figure 6-8, except connect signal generator to WHIP ANT connector J3.	
13	Repeat steps 5 through step 10.	Same as for step 10.
14	Remove jumper wire from between ANTENNA DISABLE INPUT (TB1-1) and GRD (TB1-2).	

Table 6-10. – Carrier Meter and Line Level Meter, Performance Test.

STEP	PROCEDURE	NORMAL INDICATION
1	Connect the equipment as shown in figure 6-10.	
2	Turn-on receiver and test equipment.	
3	Adjust receiver controls and switches as follows: BAND-MHZ switch: 9-17 MHz LOCK-UNLOCK control: UNLOCK TUNE control: 10 MHz FUNCTION switch: AGC M DIV TUNE-ANT DSBL switch: OFF AUDIO GAIN control: MAX RF GAIN MAX NOISE LIMITER control: OFF FINE TUNE control: 0, mid position CARRIER-OFF-LINE switch: CARRIER DETECTOR switch: AM IF BANDWIDTH switch: 2 kHz	
4	Tune signal generator frequency to center of receiver passband by tuning for a maximum indication on the RF voltmeter.	
5	Adjust signal generator output level to -88.5 dbm.	
6	Read carrier level on CARRIER-DB scale of receiver's carrier meter.	Should be 20 db
7	Adjust the signal generator output level to -70 dbm with 30% modulation at 400 Hz. Set FUNCTION switch to MGC.	
8	Adjust the receiver RF GAIN control for 0 dbm on the AF voltmeter.	
9	Switch the CARRIER-OFF-LINE switch to LINE.	0 dbm on LINE LEVEL DB meter
10	Readjust signal generator output level to the following values and observe indication on LINE LEVEL DB meter. SIGNAL GENERATOR OUTPUT LEVEL: -75, -80, -85, -90, -65 LINE LEVEL DB METER INDICATION (±2 db): -5 dbm, -10 dbm, -15 dbm, -20 dbm, +5 dbm	

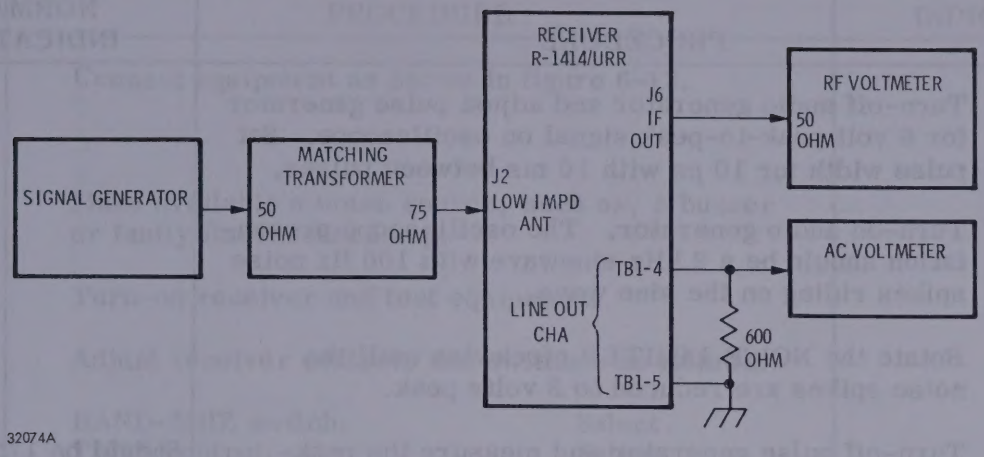


Figure 6-10. – Carrier Meter and Line Level Meter, Test Setup Diagram

Table 6-11. – Noise Suppression (Pulse Generator Method), Performance Test.

STEP	PROCEDURE	NORMAL INDICATION
1	Connect equipment as shown in figure 6-11.	
2	Disconnect the jumper between TB1-14 and TB1-15.	
3	Turn-on the receiver and test equipment.	
4	Adjust the receiver controls and switches as follows: FUNCTION switch: MGC NAR-WIDE switch: WIDE RF GAIN control: 0, full ccw DETECTOR switch: AM NOISE LIMITER control: OFF AUDIO GAIN control: MAX LINE GAIN control: MAX	
5	Adjust audio generator for an output of 2 kHz and a level of 0.35 volt rms as indicated on AC voltmeter with receiver and pulse generator disconnected.	
6	Adjust AUDIO GAIN control for 1 volt peak-to-peak signal on oscilloscope. Do this with the receiver and pulse generator connected, but with the pulse generator turned off.	

Table 6-11. – Noise Suppression (Pulse Generator Method), Performance Test - Continued.

STEP	PROCEDURE	NORMAL INDICATION
7	Turn-off audio generator and adjust pulse generator for 6 volt peak-to-peak signal on oscilloscope. Set pulse width for 10 μs with 10 ms between pulses.	
8	Turn-on audio generator. The oscilloscope presentation should be a 2 kHz sinewave with 100 Hz noise spikes riding on the sine wave.	
9	Rotate the NOISE LIMITER clockwise until the noise spikes are reduced to 3 volts peak.	
10	Turn-off pulse generator and measure the peak-to-peak voltage of the sine wave.	Should be 1/3 (approx. 1 volt) of the noise spike.
11	Reconnect the jumper between TB1-14 and TB1-15.	

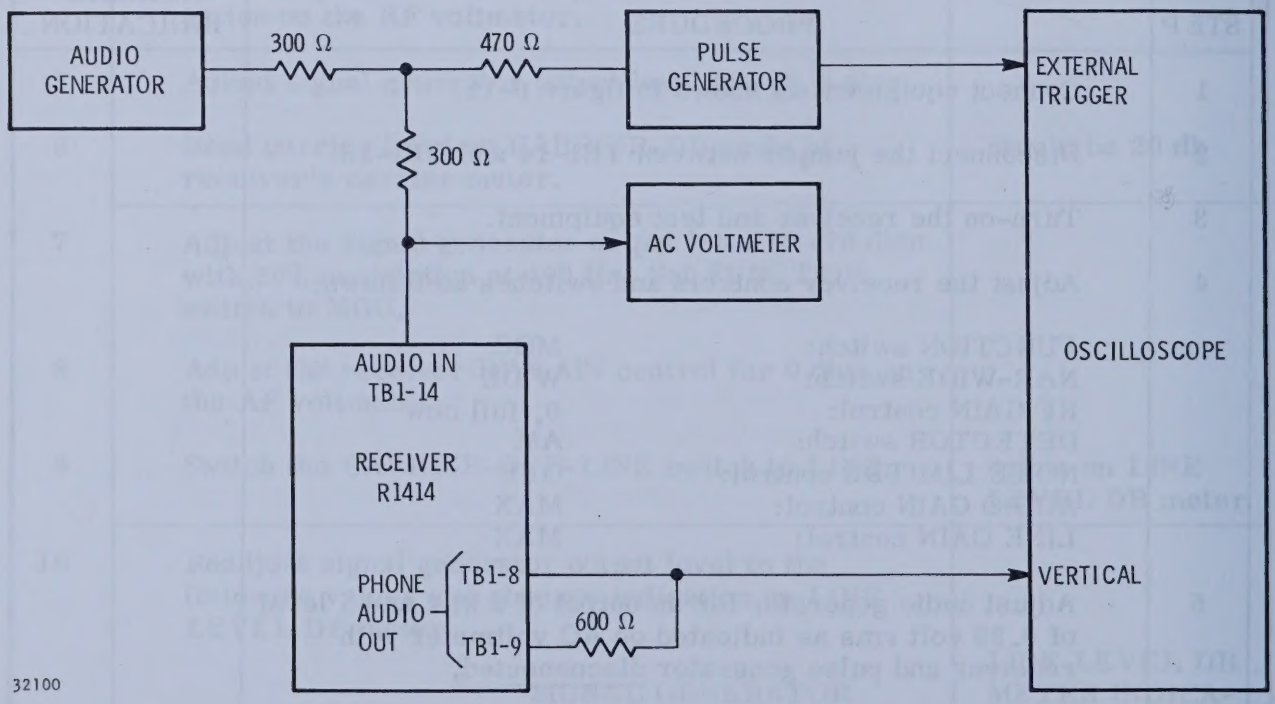


Figure 6-11. Noise Suppression, Test Setup No. 1

Table 6-12. — Noise Suppression (Noise Source Method), Performance Test.

STEP	PROCEDURE	NORMAL INDICATION
1	Connect equipment as shown in figure 6-12.	
2	Make available a noise source, such as, a buzzer or faulty fluorescent lamp.	
3	Turn-on receiver and test equipment.	
4	Adjust receiver controls and switches as follows: BAND-MHZ switch: Select TUNE control: Select FUNCTION switch: MGC NAR-WIDE switch: WIDE ANTENNA TRIM control: OFF DIV TUNE-ANT DSBL switch: OFF RF GAIN control: MAX FINE TUNE control: 0, mid-position LOCK-UNLOCK: UNLOCK BFO KHZ control: 0, mid-position DETECTOR switch: AM IF BANDWIDTH switch: 16 kHz NOISE LIMITER control: OFF AUDIO GAIN control: As Required	
5	Adjust output of signal generator for selected frequency, 400 Hz modulation of 30 percent, -99 dbm.	
6	Adjust AUDIO GAIN control for approximately 3 volts pp display on oscilloscope.	
7	Rotate the NOISE LIMITER control clockwise while observing oscillscope display.	Clockwise rotation of the NOISE LIMITER control should minimize noise while retaining maximum audio signal.

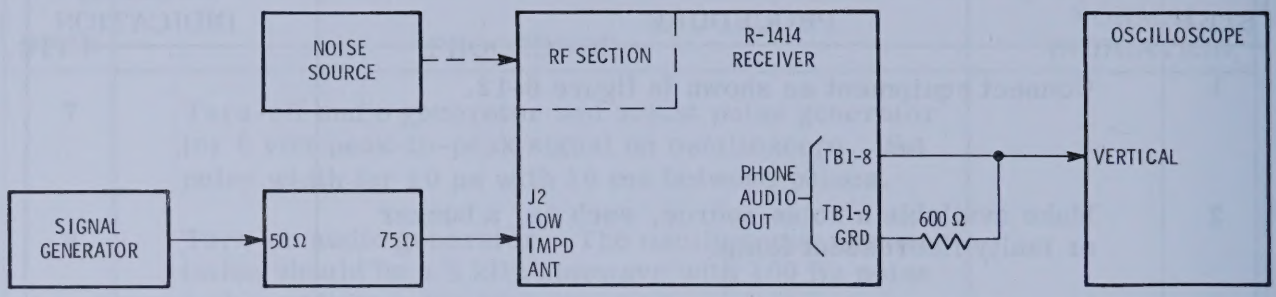


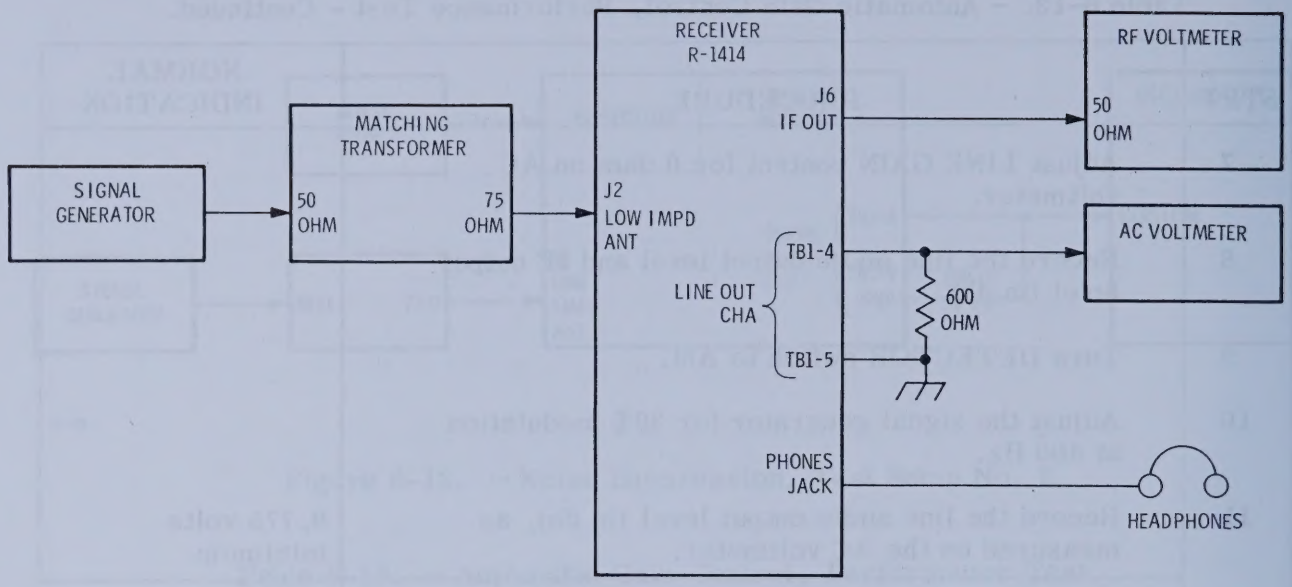
Figure 6-12. – Noise Suppression, Test Setup No. 2.

Table 6-13. – Automatic Gain Control, Performance Test.

STEP	PROCEDURE	NORMAL INDICATION
1	Connect the equipment as shown in figure 6-13.	
2	Turn-on receiver and test equipment and allow test equipment to warm-up for at least 1 hour.	
3	Adjust the receiver controls as follows: BAND-MHZ switch: 5-9 MHz TUNE control: 7.0 MHz FUNCTION switch: AGC M ANTENNA TRIM control: OFF DIV TUNE-ANT DSBL switch: OFF AUDIO GAIN control: MAX RF GAIN control: MAX FINE TUNE control: 0, mid-position LOCK-UNLOCK control: UNLOCK BFO kHz control: 0, mid-position DETECTOR switch: CW IF BANDWIDTH switch: 16 kHz NOISE LIMITER control: OFF	
4	Tune the signal generator to 7.0 MHz, and adjust its output to -99 dbm unmodulated (CW).	
5	Tune the receiver for a zero-beat in the earphones. It may be necessary to use the FINE TUNE control.	
6	Adjust the receiver BFO KHZ control to +1 kHz.	

Table 6-13. – Automatic Gain Control, Performance Test - Continued.

STEP	PROCEDURE	NORMAL INDICATION
7	Adjust LINE GAIN control for 0 dbm on AC voltmeter.	
8	Record the line audio output level and IF output level (in db)	
9	Turn DETECTOR switch to AM.	
10	Adjust the signal generator for 30% modulation at 400 Hz.	
11	Record the line audio output level (in db), as measured on the AC voltmeter.	0.775 volts minimum
12	Repeat steps 3 through step 10 with the signal generator output level adjusted to -19.0 dbm, -8.5 dbm and -88.5 dbm.	
13	Compare the levels recorded in step 8 for each of the three input levels. (This is the audio output level without signal modulation.)	There should be no more than 3 db difference in the audio level between the -88.5 and the -19.0 dbm input levels, and no more than 4 db difference in audio level between the -88.5 and -8.5 dbm input levels.
14	Compare the levels recorded in step 11 for each of the three input levels. (This is the audio output level with 400 Hz, 30% signal modulation.)	Same as for step 13.



32059A

Figure 6-13. – Automatic Gain Control, Test Setup Diagram.

Table 6-14. – BFO Range and Dial Marking Accuracy (Counter Method), Performance Test.

STEP	PROCEDURE	NORMAL INDICATION
1	Connect the equipment as shown in figure 6-14.	
2	Turn-on receiver and test equipment.	
3	Adjust receiver controls as follows:	
	BAND-MHZ switch: 5-9 MHz TUNE control: Approximately 7.0000 MHz FUNCTION switch: MGC AUDIO control: WIDE ANTENNA TRIM control: OFF DIV TUNE-ANT DSBL switch: OFF RF GAIN control MAX FINE TUNE control: 0, mid-position LOCK-UNLOCK: UNLOCK BFO KHZ control: mid-position DETECTOR switch: AM/BFO IF BANDWIDTH switch: 16 kHz NOISE LIMITER control: OFF LINE GAIN control: MAX AUDIO GAIN control: MAX	

Table 6-14. – BFO Range and Dial Marking Accuracy (Counter Method), Performance Test - Continued.

STEP	PROCEDURE	NORMAL INDICATION
4	Tune the signal generator to 7.0 MHz (±50 Hz) as indicated on receiver and adjust the output to -70 dbm, unmodulated (CW). Set DETECTOR switch to CW.	
5	Adjust the BFO KHZ control to the -8 kHz mark.	
6	Adjust RF GAIN control to obtain 0 dbm output on AC voltmeter.	The frequency counter should read 8.0 (±0.5) kHz.
7	Adjust the BFO KHZ knob to each of the following marks: -4 kHz -1 kHz +1 kHz +4 kHz +8 kHz	The frequency counter should read the frequency shown on the BFO KHZ knob ±0.5 kHz.

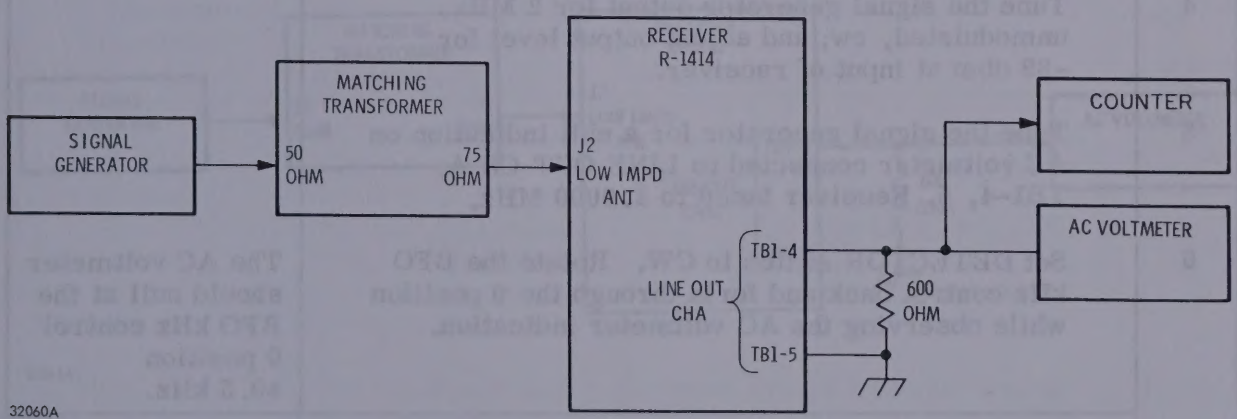


Figure 6-14. – BFO Range and Dial Marking Accuracy (Counter Method), Test Setup Diagram.

Table 6-15. – BFO Range and Dial Marking Accuracy (Zero-Beat Method), Performance Test.

STEP	PROCEDURE	NORMAL INDICATION
1	Connect equipment as shown in figure 6-15.	
2	Turn-on receiver and test equipment.	
3	Adjust receiver controls as follows: BAND-MHZ switch: 1.5-2.7 MHz TUNE control: 2.0000 MHz FUNCTION switch: MGC NAR-WIDE switch: WIDE ANTENNA TRIM control: OFF DIV TUNE-ANT DSBL switch: OFF RF GAIN control: MAX FINE TUNE control: 0, mid-position LOCK-UNLOCK UNLOCK BFO KHZ control: 0, mid-position DETECTOR switch: AM/BFO IF BANDWIDTH switch: 16 kHz NOISE LIMITER control: OFF LINE GAIN control: MAX AUDIO GAIN control: MAX	
4	Tune the signal generator output for 2 MHz, unmodulated, cw; and adjust output level for -89 dbm at input of receiver.	
5	Tune the signal generator for a null indication on AC voltmeter connected to LINE OUT CH A, TB1-4, 5. Receiver tuned to 2.0000 MHz.	
6	Set DETECTOR switch to CW. Rotate the BFO kHz control back and forth through the 0 position while observing the AC voltmeter indication.	The AC voltmeter should null at the BFO kHz control 0 position ±0.5 kHz.
7	Tune the receiver to the 2.0000 MHz minus 1 kHz. Rotate the BFO kHz control back and forth through the +1 kHz mark while observing the AC voltmeter indication. Do not change the signal generator output frequency.	The AC voltmeter should null at the BFO kHz control +1 position ±0.5 kHz.

Table 6-15. – BFO Range and Dial Marking Accuracy (Zero-Beat Method), Performance Test - Continued.

TEST	PROCEDURE	NORMAL INDICATION
8	Tune the receiver to 2.0000 MHz ± the following frequencies: +4 kHz +8 kHz -1 kHz -4 kHz -8 kHz Rotate the BFO kHz control back and forth while observing the AC voltmeter indication.	The AC voltmeter should null at the appropriate BFO kHz control position ±0.5 kHz.

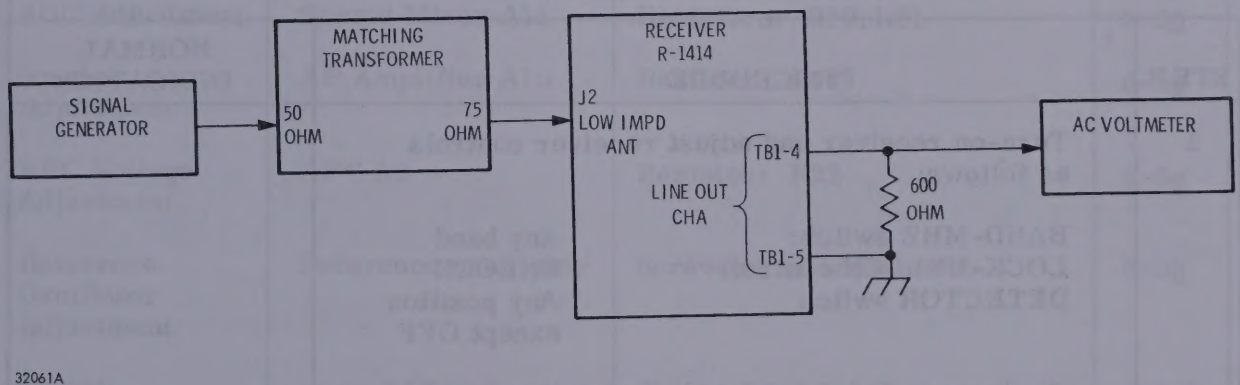


Figure 6-15. BFO Range and Dial Marking Accuracy (Zero Beat Method), Test Setup Diagram.

Table 6-16. – Dial Lock, Performance Test.

STEP	PROCEDURE	NORMAL INDICATION
1	Turn-on receiver.	
2	Adjust receiver controls as follows: BAND-MHZ switch: 17-32 MHz LOCK-UNLOCK control: UNLOCK TUNE control: Approximately 31.9990 MHz	
3	Record receiver frequency.	
4	Set the dial LOCK-UNLOCK switch to LOCK.	
5	Record the receiver frequency.	No frequency change between the recorded receiver frequencies.

Table 6-17. – Motion Detector, Performance Test.

STEP	PROCEDURE	NORMAL INDICATION
1	Turn-on receiver and adjust receiver controls as follows: BAND-MHZ switch: Any band LOCK-UNLOCK control: UNLOCK DETECTOR switch Any position except OFF	
2	Connect oscilloscope to terminal 3 (See figure 6-2.) on motion detector subassembly A1.	
3	Observe waveform on oscilloscope display as the TUNE control is rotated at different speeds.	Pulse amplitude greater than 2.8V PP. Pulse width varies from wide to narrow as rotational speed of TUNE control is increased.

6-5. ALIGNMENT AND ADJUSTMENT. - Alignment and adjustment procedures are provided as listed in table 6-18. The alignment and adjustment procedures should only be performed when it is clearly necessary; such as when a subassembly has been repaired by the removal and replacement of a defective part or when the performance test results clearly indicate that alignment or adjustment is necessary, then align only that portion required. Refer to figures 2-4, 6-1, 6-2, 6-3, 6-4, 6-5, and 6-16 for the location of alignment and adjustment controls and test points. If a complete receiver alignment and adjustment is required, start with the RFI covers removed and then install the RFI covers for final alignment and adjustment touchup.

Table 6-18. – Alignment and Adjustment Listing.

ALIGNMENT OR ADJUSTMENT	LOCATION	CONTROLS	PARA-GRAPH
RF Alignment	First local oscillator A7A1	Coils: L5,L7, L9, L10, L12 Capacitors: C21, C26, C31, C32, C37	6-5a
	Antenna tuner A1	Coils: L19, L15, L11, L7, L3 Capacitors: C7, C6, C5, C4, C3	6-5b and c
	RF tuners A2, A4, A5	Coils: L20, L16, L12, L8, L3 Capacitors: C7, C6, C5, C4, C3	6-5b and c
	First Mixer A6	Transformers: T3, T4, T5	6-5b and c
AGC Adjustment	Second Mixer A11	Resistors: R80, R81	6-5d
Squelch Adjustment	AF Amplifier A15	Resistor: R14	6-5e
AFC Voltage Adjustment	AFC A8	Resistor: R22	6-5g
Reference Oscillator Adjustment	Reference oscillator	Screwdriver adjustment	6-5h
IF Gain Adjustment	Second IF Amplifier A12	Coils: L6, L7, L9 Resistor: R31	6-5i
FM Detector Adjustment	ISB A14	Coil: L4	6-5j
2nd LO Frequency Adjustment	Second Local Oscillator	Screwdriver adjustments	6-5f
BFO Adjustment	BFO A22	Coil: L4	6-5k and l
Power Supply	Power Supply PS1 or PS2	–	6-5m

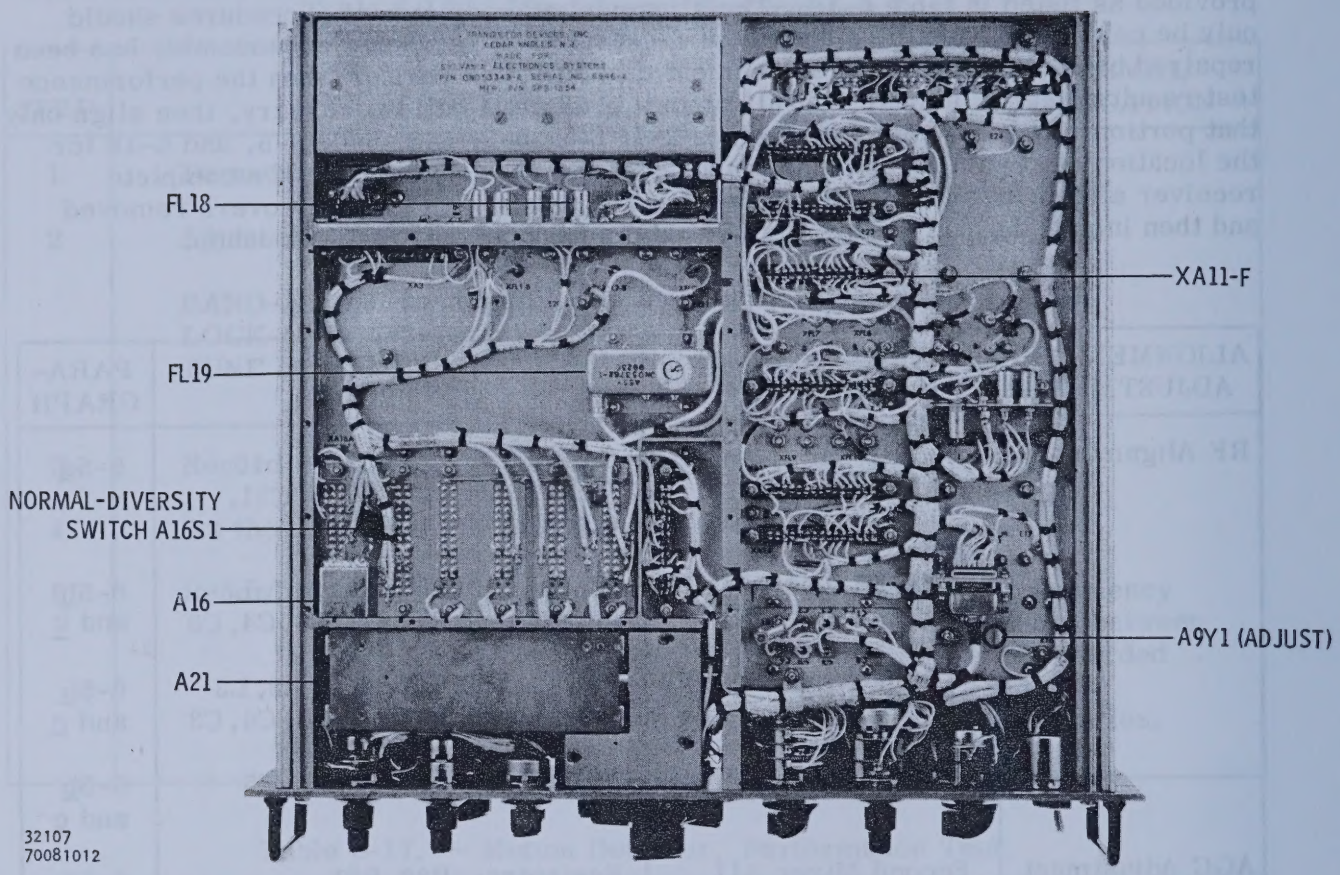


Figure 6-16. – Receiver Bottom View Identifying Test Points and Controls.

a. First Local Oscillator Alignment. - The first local oscillator, A7, is aligned using the receiver's internal frequency counter and frequency display. Refer to table 6-19 while following the alignment procedure.

(1) Connect the receiver to a power source; use no additional test equipment.

(2) Adjust the receiver LOCK-UNLOCK control.

(3) Rotate the TUNE control counterclockwise until the numbers in the FREQUENCY MHZ display no longer change. This indicates that the lowest-frequency point of the band has been reached.

(4) Select bands 1.5-2.7 through 17-32 in sequence, with the BAND-MHZ switch. In each band, tune the proper Lower Frequency Adjustment (in table 6-19) until the frequency indicated on the FREQUENCY MHZ display falls within the limits indicated as Lower Frequency.

Table 6-19. – Local Oscillator Controls.

BAND (MHz)	LOWER FREQUENCY	LOWER FREQUENCY ADJUSTMENT	UPPER FREQUENCY	UPPER FREQUENCY ADJUSTMENT
1.5-2.7	1.475-1.485	L5	2.795-2.805	C21
2.7-5	2.590-2.610	L7	5.070-5.090	C26
5-9	4.785-4.815	L9	9.205-9.235	C31
9-17	8.870-8.930	L10	17.070-17.130	C32
17-32	16.850-16.950	L12	32.350-32.450	C37

(5) Rotate the TUNE control clockwise until the numbers in the FREQUENCY MHZ display no longer change. This indicates that the highest-frequency point of the band has been reached.

(6) Select bands 1.5-2.7 through 17-32 in sequence with the BAND MHZ switch. In each band, tune the proper Upper Frequency Adjustment until the frequency indicated on the FREQUENCY MHZ display falls within the limit indicated as Upper Frequency.

(7) Since interaction exists between the Upper Frequency Adjustment and the Lower Frequency Adjustment, repeat steps (3) through (6) until all of the band-edge frequencies fall within the limits specified above.

b. RF Tuner Alignment Using HF Signal Generator. -

(1) Mixer Output Coils. - The first-mixer output coils, T3, T4, T5, must be adjusted with the mixer card, A6, on a card extender. For location of the coils, see figures 6-1 and 6-2.

(a) Connect the receiver and test equipment as shown in figure 6-8, except for the attenuator.

(b) Adjust the receiver controls as follows:

BAND-MHZ:	1.5-2.7
LOCK-UNLOCK	UNLOCK
TUNE:	2.0000 MHz
FINE TUNE:	0, mid-position

FUNCTION:	MGC
IF BANDWIDTH:	2 kHz
DETECTOR:	AM
ANTENNA TRIM:	OFF
DIV TUNE-ANT DSBL:	OFF
RF GAIN:	MAX

(c) Adjust the signal generator output to -10 dbm.

(d) Tune the signal generator back and forth across the receiver passband until the IF output voltage is at a maximum. The signal generator should now be tuned to the center of the receiver passband.

(e) Reduce the signal generator output to -99.0 dbm (2.5μv), as indicated at signal generator.

(f) Adjust T3 for a maximum IF output level.

(g) Repeat steps (a) through (e) for receiver and signal generator frequencies of 4.0000 MHz and 10.0000 MHz. Adjust T4 at 4.0000 MHz, and T5 at 10.0000 MHz, for maximum IF output.

(2) RF Tuners. - The RF tuners, A1, A2, A4, and A5, are aligned together. Refer to the following table 6-20 while following the alignment procedure. (see figures 6-1 and 6-2) Repeat procedure as necessary, approximately five times.

Table 6-20. - RF Tuner Controls and IF Bandwidth

		A1		A2, A4, A5	
BAND	IF BANDWIDTH	LOWER ADJUSTMENT	UPPER ADJUSTMENT	LOWER ADJUSTMENT	UPPER ADJUSTMENT
1.5-2.7	2 kHz	L19	C7	L20	C7
2.7-5	2 kHz	L15	C6	L16	C6
5-9	6 kHz	L11	C5	L12	C5
9-17	6 kHz	L7	C4	L8	C4
17-32	16 kHz	L3	C3	L3	C3

(a) Connect the receiver and test equipment as shown in figure 6-8 except for the attenuator.

(b) Adjust the receiver controls as follows:

LOCK-UNLOCK	UNLOCK
FINE TUNE:	0, mid-position
FUNCTION:	MGC

DETECTOR:	AM
ANTENNA TRIM:	OFF
DIV TUNE-ANT DSBL:	OFF
RF GAIN:	MAX

(c) Set the BAND-MHZ switch and the IF BANDWIDTH switch, following the table above. Beginning with 1.5-2.7 MHz and 2 kHz, adjust the appropriate components using the procedure described in steps (d) through (n) below: then repeat the procedures, referring to table 6-20 for each of the other BAND-MHZ switch positions.

(d) Adjust the signal generator output to 1 mv (-47 dbm), as indicated at signal generator.

(e) Rotate the TUNE control counterclockwise until the numbers in the FREQUENCY MHZ display no longer change. This indicates that the lowest-frequency point of the band has been reached.

(f) Tune the signal generator back and forth across the receiver passband until the IF output voltage is at a maximum. The signal generator should now be tuned to the center of the receiver passband.

(g) Reduce the signal generator output to -99.0 dbm (2.5μv).

(h) Adjust the appropriate inductors listed under the Lower Adjustment columns of table 6-20 for maximum IF output. Note that the first lower adjustment column lists the inductors to be adjusted on A1, while the second Lower Adjustment column lists the adjustments on A2, A4, and A5.

(i) Rotate the TUNE control clockwise until the numbers in the FREQUENCY MHZ display no longer change. This indicates that the highest-frequency point of the band has been reached.

(j) Adjust the signal generator output to 1 mv (-47 dbm).

(k) Tune the signal generator back and forth across the receiver passband until the IF output voltage is at a maximum. The signal generator should now be tuned to the center of the receiver passband.

(l) Reduce the signal generator output to a level which does not over driver any stages within the receiver (-99.0 dbm is typical).

(m) Adjust the appropriate capacitors listed under the Upper Adjustment columns of table 6-20 for maximum IF output.

(n) Due to interaction of the Lower Adjustment and the Upper Adjustment, steps (d) through (m) must be repeated until no further adjustments are required to obtain a maximum IF output.

c. RF Tuner Alignment Using Sweep Generator. -

(1) Mixer Output Coils. - Refer to paragraph 6-5b(1).

(2) RF Tuners. - The RF tuners A1, A2, A4, and A5 are aligned together. Refer to table 6-21 while following the alignment procedure (see figures 6-1 and 6-2).

Table 6-21. - RF Tuner Controls.

	A1		A2, A4, A5	
BAND	LOWER ADJUSTMENT	UPPER ADJUSTMENT	LOWER ADJUSTMENT	UPPER ADJUSTMENT
1.5-2.7	L19	C7	L20	C7
2.7-5	L15	C6	L16	C6
5-9	L11	C5	L12	C5
9-17	L7	C4	L8	C4
17-32	L3	C3	L3	C3

(a) Connect receiver and test equipment as shown in figure 6-17.

(b) Adjust receiver controls as follows:

LOCK-UNLOCK control:	UNLOCK
ANTENNA TRIM control:	OFF
DIV TUNE-ANT DSBL switch:	OFF

(c) Set the NORMAL-DIVERSITY switch (located on bottom of receiver, see figure 6-16) to DIVERSITY.

(d) Beginning with BAND-MHZ switch position 1.5-2.7, adjust the appropriate components using the procedure described in the following steps (e) through (l); then repeat the procedure for each of the other BAND-MHZ switch positions while referring to table 6-21.

(e) Condition signal generator, sweep generator, and oscilloscope for a bandpass display centered on oscilloscope face. The attenuator between the signal generator and the sweep generator may be needed to properly superimpose the marker on the bandpass display.

(f) Rotate the TUNE control counterclockwise until the FREQUENCY MHZ digital display indicates the lower band edge frequency (this would be 1.5 MHz for the 1.5-2.7 frequency band).

(g) Tune the signal generator output frequency for the lower band edge frequency.

(h) Adjust A1L19 and A2L20, A4L20, and A5L20 as listed in table 6-21, for a symmetrical response at maximum amplitude as indicated on oscilloscope.

(i) Rotate the TUNE control clockwise until the FREQUENCY MHZ digital display indicates the upper band edge frequency (this would be 2.7 MHz for the 1.5-2.7 frequency band).

(j) Tune the signal generator output frequency for the upper band edge frequency.

(k) Adjust C7 and A1, A2, A4, and A5 as listed in table 6-21, for a symmetrical response at maximum amplitude as indicated on oscilloscope.

(1) Due to interaction of the lower and upper frequency adjustments, steps (f) through (k) may need to be repeated.

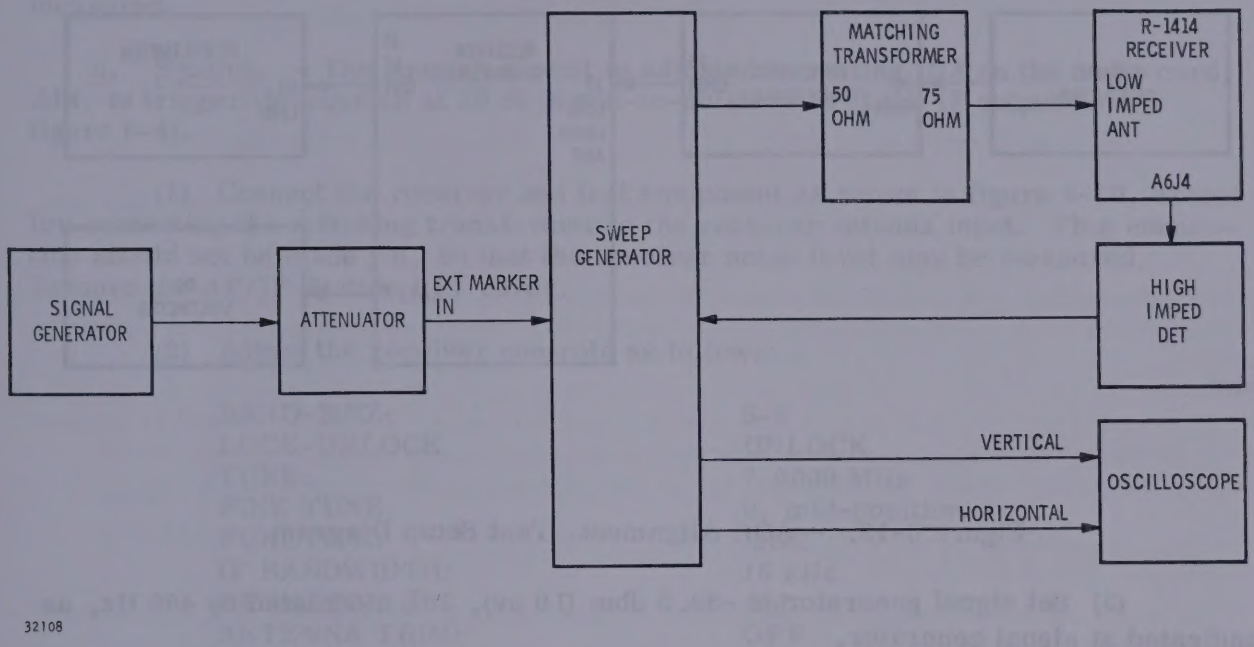


Figure 6-17. – RF Tuner Alignment (Sweep Generator), Test Setup Diagram.

d. Automatic Gain Control. - The AGC is aligned by adjusting the printed-circuit-card-mounted potentiometers, R80 and R81, located on the second mixer card, A11 (see figure 6-4).

(1) Connect the receiver and test equipment as shown in figure 6-18. Note that the dc voltmeter must be connected to pin F of XA11. To gain access to this point, remove the receiver bottom cover.

(2) Adjust the receiver controls as follows:

BAND-MHZ:	5-9
LOCK-UNLOCK:	UNLOCK
TUNE:	7.0000 MHz
FINE TUNE:	0, mid-position
FUNCTION:	MGC
IF BANDWIDTH:	16 kHz
DETECTOR:	AM
ANTENNA TRIM:	OFF
DIV TUNE-ANT DSBL:	OFF
RF GAIN:	MAX

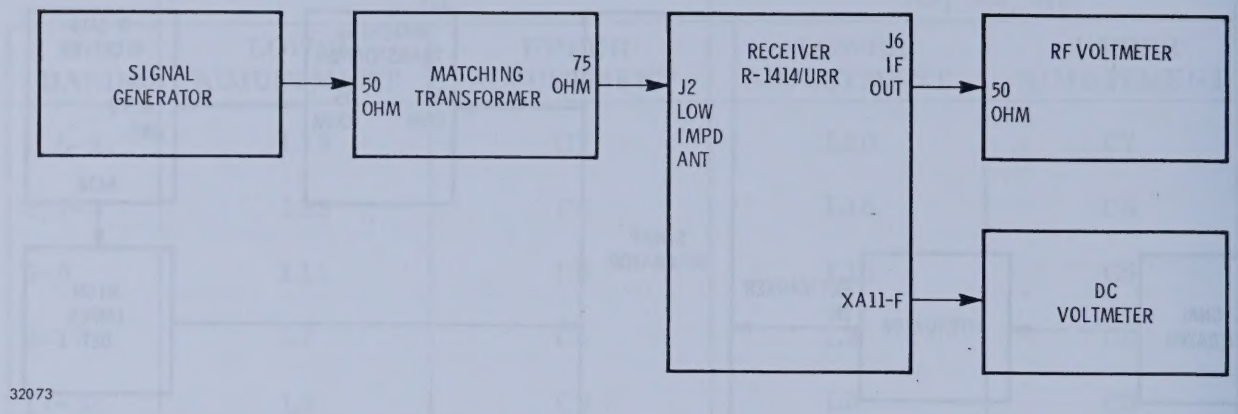


Figure 6-18. – AGC Alignment, Test Setup Diagram.

(3) Set signal generator to -88.5 dbm (10 μv), 30% modulated by 400 Hz, as indicated at signal generator.

(4) Tune the signal generator to the center of the receiver passband. Adjust R80 and R81 full clockwise.

(5) Adjust the RF GAIN control to give a 12.0 vdc reading on the dc voltmeter.

(6) Short the FL18 feed through capacitor to ground using a jumper wire (see figure 6-16 for location).

(7) Increase the signal generator output until a 30 millivolt reference is measured by the RF voltmeter. Record signal generator level in dbm.

(8) Remove jumper wire from capacitor FL18.

(9) Increase the signal generator output by 20 db. Record signal generator level in dbm.

(10) Adjust R80 until the 30 mv reference again is measured.

(11) Set RF GAIN to maximum counterclockwise.

(12) Short FL18 to ground and record the voltage measured by the RF voltmeter.

(13) Remove the jumper wire from FL18.

(14) Increase the signal generator output by 30 db, over the recorded value in step 9.

(15) Adjust R81 until the recorded voltage measured in step 12 is again measured.

e. Squelch. - The squelch circuit is adjusted by setting R14 on the audio card, A14, to trigger the squelch at 20 db signal-to-noise ratio at the IF output (see figure 6-4).

(1) Connect the receiver and test equipment as shown in figure 6-10, except for connecting the matching transformer to the receiver antenna input. This connection should not be made yet, so that the receiver noise level may be measured. Remove the AF/IF Section RFI cover.

(2) Adjust the receiver controls as follows:

BAND-MHZ:	5-9
LOCK-UNLOCK	UNLOCK
TUNE:	7.0000 MHz
FINE TUNE:	0, mid-position
FUNCTION:	MGC
IF BANDWIDTH:	16 kHz
DETECTOR:	AM
ANTENNA TRIM:	OFF
DIV TUNE-ANT DSBL:	OFF
RF GAIN:	MAX
NOISE LIMITER:	OFF

(3) Establish a noise level reference at the IF output by noting the reading on the RF voltmeter.

(4) Adjust the signal generator to 30% modulation at 400 Hz.

(5) Connect the matching transformer to the receiver LOW-IMPD ANT input.

(6) Adjust the signal generator output level to obtain an RF volmeter reading 20 db higher than the reference level noted in step (3).

(7) Set FUNCTION switch to SQUELCH.

(8) Beginning with R14 adjusted full counterclockwise, adjust R14 clockwise until the line audio output, measured by the AF voltmeter, just jumps up suddenly (by about 15 db).

(9) Replace the AF/IF RFI cover.

f. Second Local Oscillator A18. - The three frequency outputs from the second local oscillator may be checked at test point J2 of A11 using a frequency counter and RF voltmeter. The outputs should be as follows:

(1) Band 1.5-2.7, 847 kHz (±30 Hz), 0.8 to 1.2 volts rms

(2) Bands 2.7-5 and 5-9, 1217 kHz (±20 Hz), 0.8 to 1.2 volts rms

(3) Bands 9-17 and 17-32, 3217 kHz (±15 Hz), 0.8 to 1.2 volts rms

Note: – Do not make any adjustments unless the output frequencies are not within tolerance.

If the outputs are not within tolerance, remove protective cover and adjust the appropriate screwdriver control on the second local oscillator (see figure 6-4) for correct output.

g. AFC A8. - The AFC voltage at test point J1 of AFC circuit board A8 should be 7.3 (±1.5) vdc when the receiver is tuned to a signal and it should be stable to within ±0.2 vdc. When the AFC voltage is out-of-tolerance proceed as follows:

(1) Adjust R22 on A8 for 7.3 (±0.2) vdc as indicated on a DC voltmeter connected to test point A8J1.

(2) Disable motion detector circuit by turning the LOCK-UNLOCK control to LOCK and observe rate of drift on voltmeter.

(3) If AFC voltage is increasing, adjust R22 clockwise. If AFC voltage is decreasing, adjust R22 counterclockwise. Adjust until reasonably stable to within ±0.2 vdc.

Note: – If the drift should be extreme before R22 is properly adjusted, enable the AFC and adjust AFC voltage to 7.3 (±0.2) volts.

h. RF Oscillator A9Y1. - The RF oscillator A9Y1 in the counter provides a 1 MHz reference signal to the gate generator. The RF oscillator output is extremely stable and may never require adjustment. The oscillator output can be checked by installing the gate generator board on a card extender. Connect a frequency counter to pin C on gate generator and check oscillator output frequency. The output frequency should be 1 MHz (±0.3 Hz). Connect an oscilloscope using X1 probe to pin C on gate generator and observe 2.9 (±1)V pp waveform. If the frequency output is not within tolerance, remove plastic cover and adjust screwdriver control (see figure 6-16 for 1 MHz) (±0.3 Hz) output on frequency counter.

i. Second IF Amplifier A12. - The second IF amplifier board A12 contains coils L6, L7, and L9; and resistor R31 that are adjustable as follows:

(1) Connect signal generator and RF voltmeter as shown in figure 6-10.

(2) Remove dust cover and AF/IF section RFI cover.

(3) Install second IF amplifier board A12 (see figure 6-4) on an extender board.

(4) Turn-on receiver and test equipment.

(5) Adjust receiver controls as follows:

BAND-MHZ switch:	As required.
TUNE control:	As required.
FUNCTION switch:	MGC
ANTENNA TRIM control:	OFF
DIV TUNE-ANT DSBL switch;	OFF
RF GAIN control:	MAX
FINE TUNE control:	0, mid-position
LOCK-UNLOCK control:	UNLOCK
BFO KHZ control:	mid-position
DETECTOR switch:	CW
IF BANDWIDTH switch:	6 kHz

(6) Tune signal generator and receiver for the least sensitive receiver frequency (usually 32 MHz) as established in table 6-6.

(7) Adjust signal generator output for -99 dbm (2.5 μv) and unmodulated

(8) Adjust coils L6, L7, and L9 (see figure 7-15) for maximum response on RF voltmeter.

(9) Remove board A12 from extender board on reinstall in receiver.

(10) Adjust resistor R31 (see figure 6-4) for 30 mv indication on RF voltmeter.

j. ISB A14. - Adjust coil L4 on ISB board A14 as follows:

(1) Install ISB on an extender board.

(2) Connect FM signal generator to antenna input and AC voltmeter to LINE OUT CH A as shown in figure 6-9.

(3) Set the DETECTOR switch to FM.

(4) Set CH A LINE GAIN to MAX.

(5) Set IF BANDWIDTH switch to 16 kHz.

(6) Set BAND-MHZ switch to the selected frequency band.

(7) Condition signal generator for 5.6 kHz deviation at 1 kHz rate.

(8) Adjust signal generator and receiver to the same frequency.

(9) Set signal generator output level for -99 dbm at input of receiver.

(10) Adjust coil L5 (see figure 7-13) for a peak on AC voltmeter.

k. BFO KHZ Control Centering and Accuracy (frequency counter method). - Center BFO KHZ knob and adjust L4 on BFO board A22 as follows:

(1) Loosen set screws on BFO KHZ knob.

(2) Position knob on shaft so that the pointer travels the same distance past +8 and -8 when tuning full cw and ccw.

(3) Tighten set screws and recheck knob centering.

(4) Connect a frequency counter to test jack J4 (see figure 6-4) on ISB board A14.

(5) Tune BFO KHZ knob to +8.

(6) Set DETECTOR switch to CW.

(7) Pull BFO board A22 (see figure 1-2) up from chassis to limit of wiring travel.

(8) Adjust L4 on A22 to indicate 463.0 kHz on frequency counter.

(9) Replace BFO board A22 in chassis.

(10) Replace BFO cover and check BFO accuracy over entire range.

l. BFO KHZ Knob Centering and Accuracy (Zero beat method). - Center BFO KHZ control and adjust L4 on BFO board A22 as follows:

(1) Loosen set screws on BFO KHZ control.

(2) Position control on shaft so that the pointer travels the same distance past the +8 and -8 when rotation full cw and ccw.

(3) Tighten set screws and recheck the BFO KHZ control centering.

(4) Connect equipment as shown in figure 6-8, except for attenuator.

(5) Turn-on receiver and test equipment.

(6) Adjust receiver controls as follows:

BAND-MHZ switch:	1.5-2 MHz
TUNE control:	2.0000 MHz
FUNCTION switch:	MGC
NAR-WIDE switch:	WIDE

ANTENNA TRIM control:	OFF
DIV TUNE-ANT DSBL switch:	OFF
RF GAIN control:	MAX
FINE TUNE control:	0, mid-position
LOCK-UNLOCK:	UNLOCK
BFO KHZ control:	0, mid-position
DETECTOR switch:	AM/BFO
IF BANDWIDTH switch:	16 kHz
NOISE LIMITER control:	OFF
LINE GAIN control:	MAX
AUDIO GAIN control:	MAX

(7) Tune the signal generator output for 2 MHz, unmodulated, cw; and adjust output level for -89 dbm at input of receiver.

(8) Tune the signal generator for a null indication on AC voltmeter connected to LINE OUT CH A, TB1-4. Adjust RF GAIN control as necessary.

(9) Set DETECTOR switch to CW.

(10) Tune the receiver to 1.9920 MHz.

(11) Adjust BFO KHZ control to +8.

(12) Pull BFO board A22 (see figure 1-2) up from chassis to limit of wiring travel.

(13) Adjust L4 on A22 for a null indication on AC voltmeter connected to LINE OUT CH A, TB1-4, -5.

(14) Replace BFO board A22 in chassis.

(15) Rotate the BFO KHZ control back and forth through the +8 position while observing the AF voltmeter indication. The AC voltmeter should null at the +8 position ±0.5 kHz. Replace BFO cover and check BFO accuracy throughout its entire range.

(16) If still out-of-tolerance repeat steps 10 through 13 for a slightly different adjustment of L4 on BFO board A22.

m. Power Supply Adjustment. - The output voltages for ac input power supply PS1 and the dc input power supply PS2 are adjusted at each regulator by the selection of taps on a resistor divider network.

(1) Adjust of +5 VDC Regulator. - The +5 vdc regulator output is normally set for +5 (±0.2) vdc at full load with minimum input voltage. Resistors R20 and R21 are the voltage trimming resistors. Jumpering terminals E27 to E31 increases the output voltage approximately 0.5 percent. Jumpering terminals E28 to E31 increases the output voltage by approximately 1 percent. Jumpering terminals E27 to E32 lowers the output voltage by approximately 3 percent.

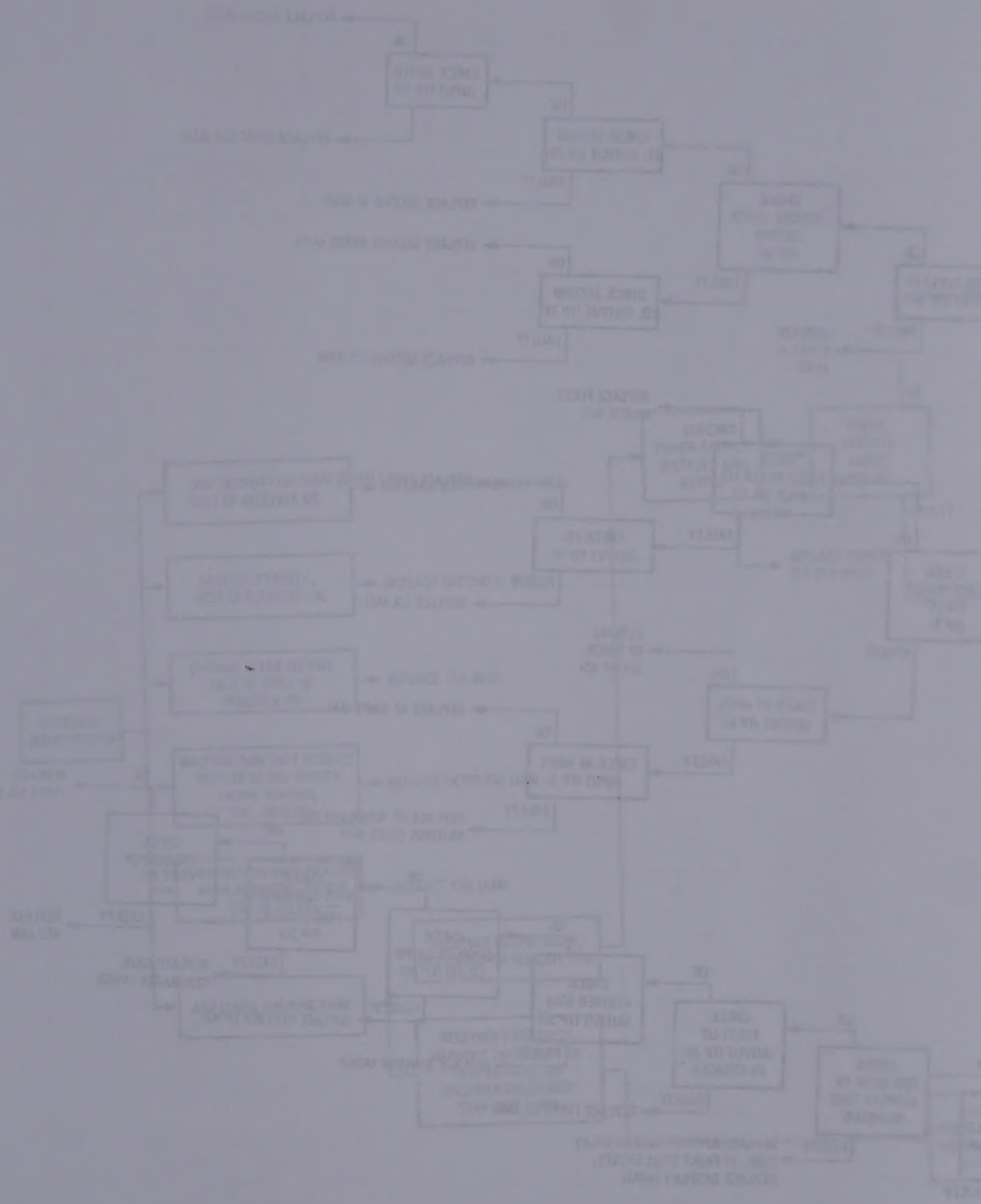
(2) Adjustment of +230 VDC Regulator. - The +230 vdc regulator output is normally set for +230 (±15) vdc at full load with minimum input voltage. Resistors R7 and R10 are the voltage trimming resistors. Resistor R9 may be shorted out by a jumper from terminal E33 to E34, which will decrease the output voltage by approximately 5 percent. Resistor R10 may be shorted out by a jumper from E21 to E34, which will decrease the output voltage by approximately 10 percent. Both resistors R9 and R10 may be shorted out, which will decrease the output voltage by approximately 15 percent.

(3) Adjustment of -8 VDC Regulator. - The -8 vdc regulator output is normally -8 (±0.2) vdc at full load with minimum input voltage. Resistors R25 and R26 are the voltage trimming resistors. Jumpering terminals E30 and E35 decreases the output voltage by approximately 2 percent. Jumpering terminals E29 and E38 increases the output voltage by approximately 1.5 percent. Jumpering terminals E30 and E38 increases the output voltage by approximately 3 percent.

(4) Adjustment of +25 VDC Regulator. - The +25 vdc regulator output is normally +25 (±0.4) vdc at full load with minimum input voltage. Resistors R15 and R16 are the voltage trimming resistors. Jumpering terminals E33 and E36 decreases the output voltage by approximately 3 percent. Jumpering terminals E34 and E36 decreases the output voltage by approximately 1 percent. Jumpering terminals E33 and E37 increases the output voltage by approximately 1.5 percent.

6-6. GENERAL TROUBLESHOOTING INFORMATION. - When troubleshooting the receiver, first try to locate a malfunction by sectionalizing the fault to a functional area like the RF section, counter section, etc. The next step is to localize a fault to a defective subassembly; such as a plug-in type printed circuit board or to parts and wiring of the front panel or main frame. If the fault has been localized to a printed circuit, further localization to a stage or component can be accomplished by visual inspection, use of performance tests, or by use of voltage, resistance, and continuity measurements. Some faults such as burned-out resistors, shorted transformers, and loose connections often can be located by sight, smell, and hearing. The majority of faults, however, must be located by performance, voltage, and resistance checks. In many cases, the performance tests will help in determining the exact nature of the fault. The receiver performance tests should first be performed and all trouble symptoms recorded. The tests and troubleshooting procedures should then be performed.

6-7. TROUBLESHOOTING. - The receiver troubleshooting charts (see figures 6-19, 6-20, and 6-21) present information to trace troubles to a faulty subassembly. For best results, first perform the receiver performance tests and record all trouble symptoms prior to using the troubleshooting charts. If the trouble has been isolated to a chassis mounted component or wiring, replace component or wiring and then check for performance. If the trouble has been isolated to a replaceable subassembly, perform visual checks and then perform the appropriate testing procedures for that subassembly to isolate a malfunction to a component or group of components. Voltage and resistance checks can then be performed for further isolation. Before replacing a component, ensure that there is no break in continuity that would cause the malfunction at that location. Refer to figures 6-1 through 6-5 for views of the RF section, counter section, IF section, and power supply identifying the location of all test points



(2) Adjustment of +230 VDC Regulator. - The +230 vdc regulator output is normally set for +230 (±15) vdc at full load with minimum input voltage. Resistors R7 and R10 are the voltage trimming resistors. Resistor R9 may be shorted out by a jumper from terminal E33 to E34, which will decrease the output voltage by approximately 5 percent. Resistor R10 may be shorted out by a jumper from E21 to E34, which will decrease the output voltage by approximately 10 percent. Both resistors R9 and R10 may be shorted out, which will decrease the output voltage by approximately 15 percent.

(3) Adjustment of -8 VDC Regulator. - The -8 vdc regulator output is normally -8 (±0.2) vdc at full load with minimum input voltage. Resistors R25 and R26 are the voltage trimming resistors. Jumpering terminals E30 and E35 decreases the output voltage by approximately 2 percent. Jumpering terminals E29 and E38 increases the output voltage by approximately 1.5 percent. Jumpering terminals E30 and E38 increases the output voltage by approximately 3 percent.

(4) Adjustment of +25 VDC Regulator. - The +25 vdc regulator output is normally +25 (±0.4) vdc at full load with minimum input voltage. Resistors R15 and R16 are the voltage trimming resistors. Jumpering terminals E33 and E36 decreases the output voltage by approximately 3 percent. Jumpering terminals E34 and E36 decreases the output voltage by approximately 1 percent. Jumpering terminals E33 and E37 increases the output voltage by approximately 1.5 percent.

6-6. GENERAL TROUBLESHOOTING INFORMATION. - When troubleshooting the receiver, first try to locate a malfunction by sectionalizing the fault to a functional area like the RF section, counter section, etc. The next step is to localize a fault to a defective subassembly; such as a plug-in type printed circuit board or to parts and wiring of the front panel or main frame. If the fault has been localized to a printed circuit, further localization to a stage or component can be accomplished by visual inspection, use of performance tests, or by use of voltage, resistance, and continuity measurements. Some faults such as burned-out resistors, shorted transformers, and loose connections often can be located by sight, smell, and hearing. The majority of faults, however, must be located by performance, voltage, and resistance checks. In many cases, the performance tests will help in determining the exact nature of the fault. The receiver performance tests should first be performed and all trouble symptoms recorded. The tests and troubleshooting procedures should then be performed.

6-7. TROUBLESHOOTING. - The receiver troubleshooting charts (see figures 6-19, 6-20, and 6-21) present information to trace troubles to a faulty subassembly. For best results, first perform the receiver performance tests and record all trouble symptoms prior to using the troubleshooting charts. If the trouble has been isolated to a chassis mounted component or wiring, replace component or wiring and then check for performance. If the trouble has been isolated to a replaceable subassembly, perform visual checks and then perform the appropriate testing procedures for that subassembly to isolate a malfunction to a component or group of components. Voltage and resistance checks can then be performed for further isolation. Before replacing a component, ensure that there is no break in continuity that would cause the malfunction at that location. Refer to figures 6-1 through 6-5 for views of the RF section, counter section, IF section, and power supply identifying the location of all test points

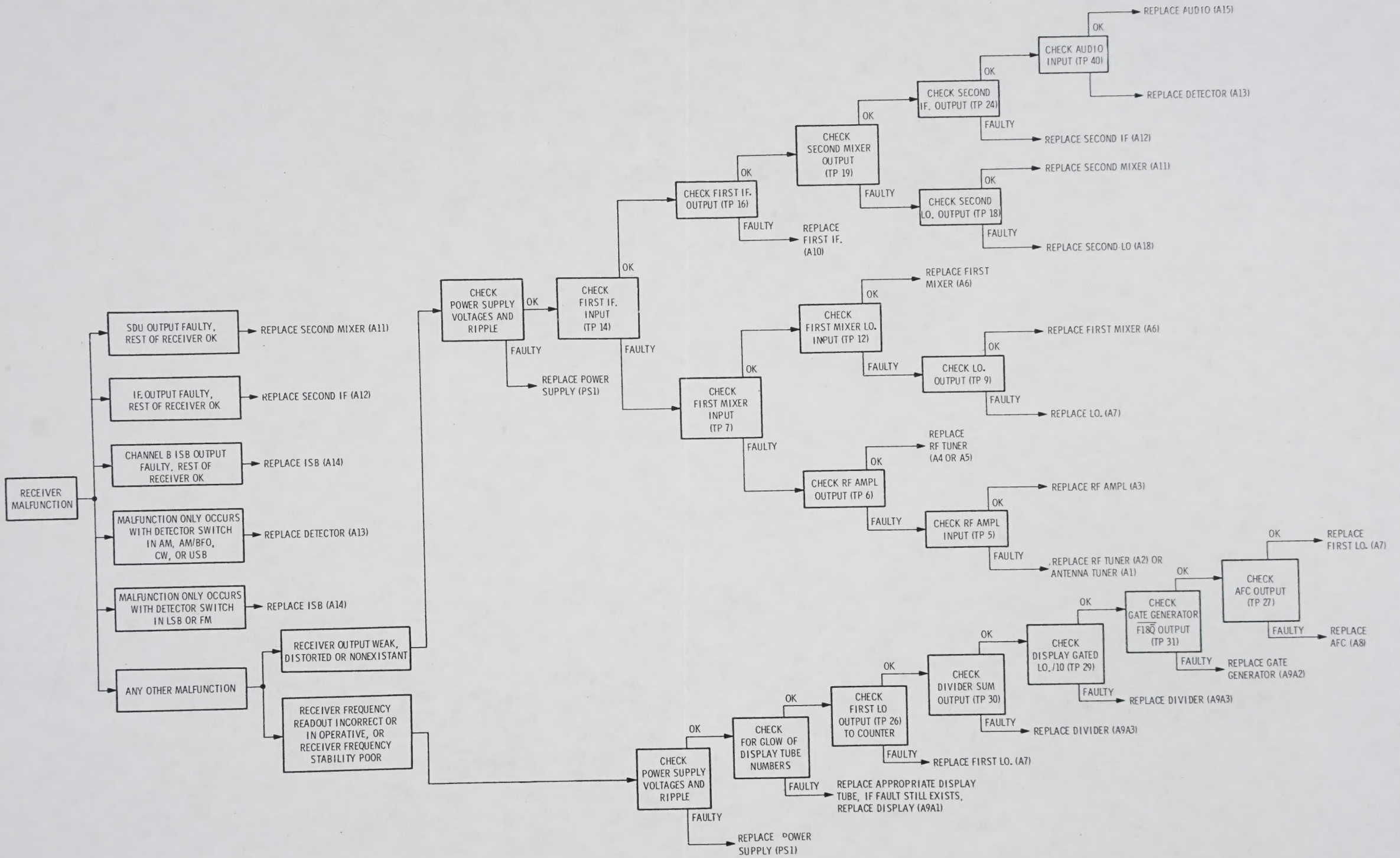


Figure 6-19. – Receiver Troubleshooting Chart.

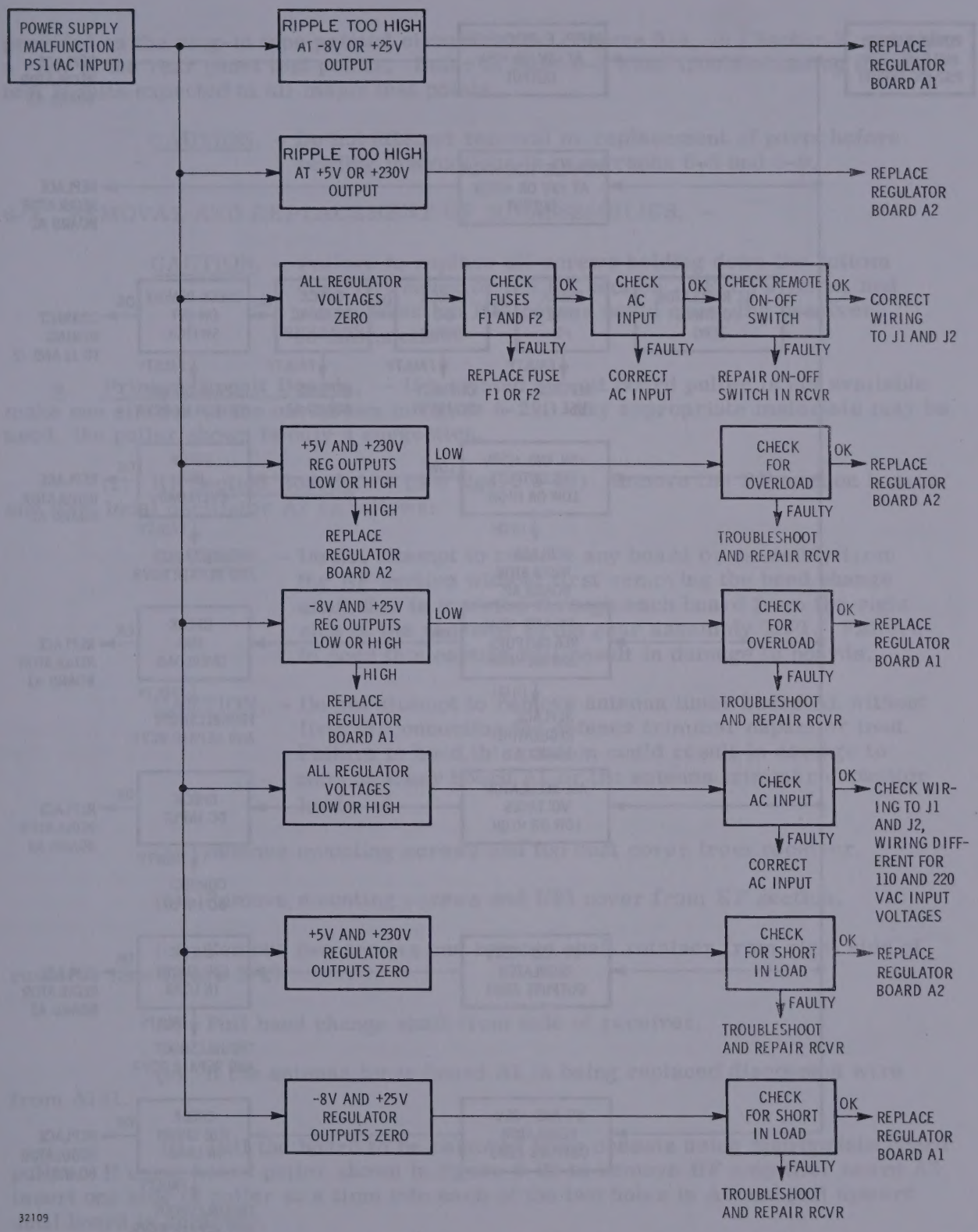


Figure 6-20. – AC Input Power Supply, Troubleshooting Chart.

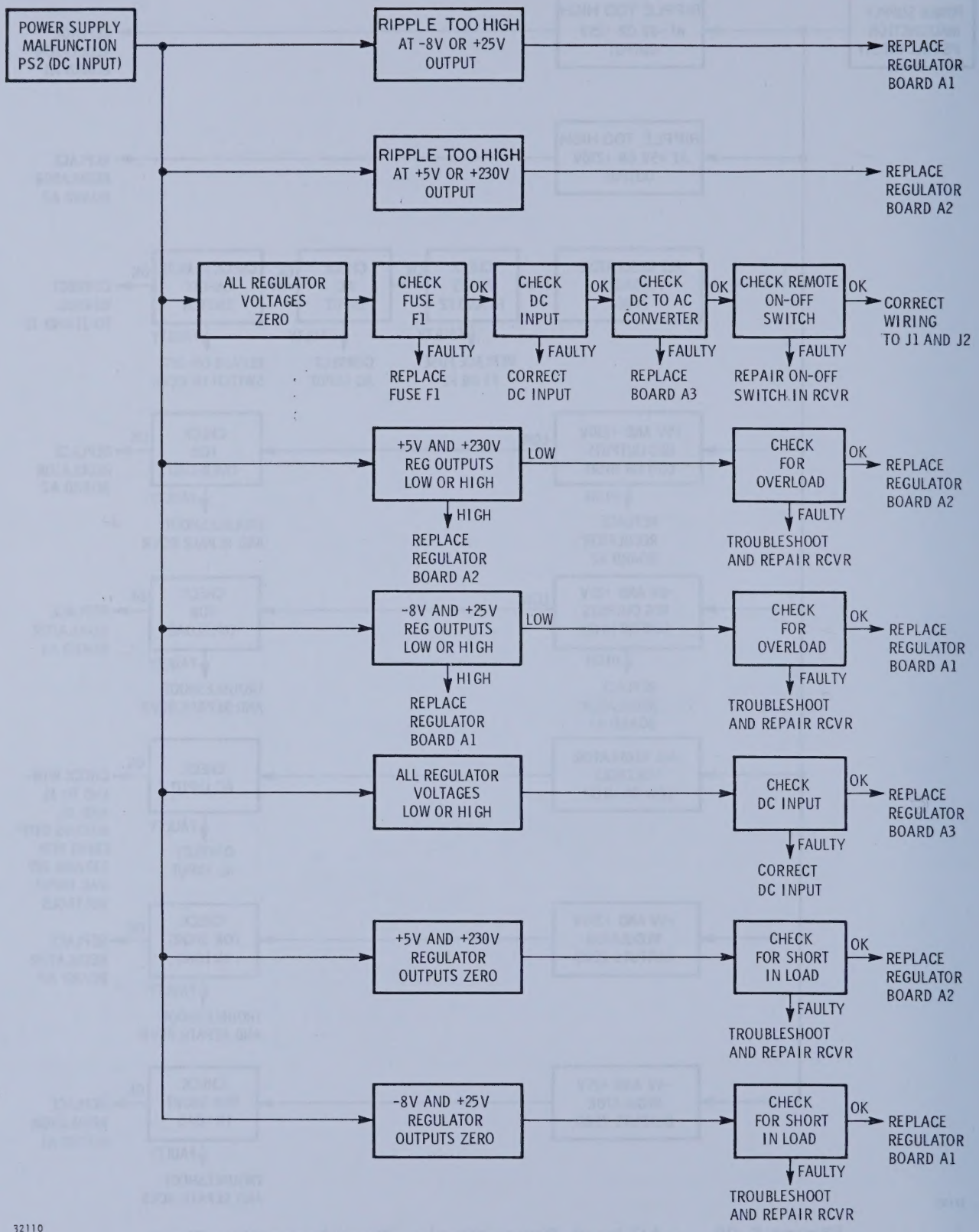


Figure 6-21. DC Input Power Supply, Troubleshooting Chart.

provided on the plug-in type printed circuit cards. Figure 2-4, in Chapter 2, provides a view of the rear panel test points. Refer to table 6-3 when troubleshooting for the test results expected at all major test points.

CAUTION. - Do not attempt removal or replacement of parts before reading instructions in paragraphs 6-8 and 6-9.

6-8. REMOVAL AND REPLACEMENT OF SUBASSEMBLIES. -

CAUTION. - Failure to replace all screws holding down the bottom dust/RFI cover or the RF section, AF/IF section, and counter section RFI covers could cause the receiver to malfunction.

a. Printed Circuit Boards. - If a printed circuit board puller is not available make one similar to the one shown in figure 6-22. Any appropriate materials may be used, the puller shown is only a suggestion.

(1) RF Section Boards. - (See figure 6-2.) Remove the RF section boards and first local oscillator A7 as follows:

CAUTION. - Do not attempt to remove any board or assembly from the RF section without first removing the band change shaft that is inserted through each board from the right side of the receiver to the gear assembly MP1. Failure to heed this caution will result in damage to boards.

CAUTION. - Do not attempt to remove antenna tuner board A1 without first disconnecting the antenna trimmer capacitor lead. Failure to heed this caution could result in damage to antenna tuner board A1 or the antenna trimmer capacitor lead.

(a) Remove mounting screws and top dust cover from receiver.

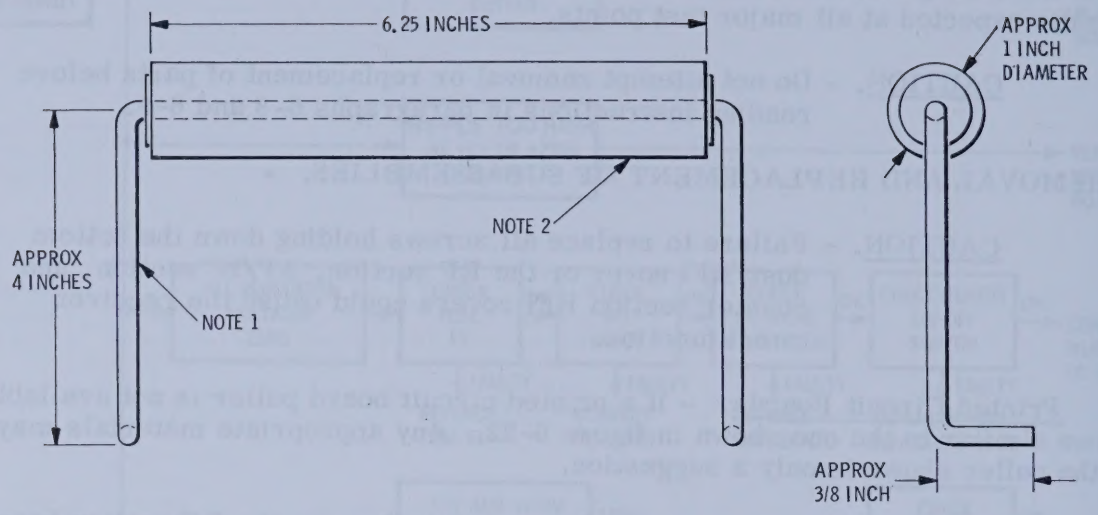
(b) Remove mounting screws and RFI cover from RF section.

(c) Remove two screws and remove shaft retainer from right side of receiver (See figure 2-2).

(d) Pull band change shaft from side of receiver.

(e) If the antenna tuner board A1 is being replaced disconnect wire from A1J1.

(f) Pull the board to be removed from chassis using appropriate board puller. If using board puller shown in figure 6-22 to remove RF amplifier board A3, insert one side of puller at a time into each of the two holes in A3 and pull upward until board is removed.



NOTES:

1. USE 0.125 INCH STAINLESS STEEL BAR TYPE 303, FEDERAL SPECIFICATION QQ-S-763 OR ANY SUBSTITUTE BAR STOCK, SUCH AS, 0.125 INCH WELDING ROD
2. PREPARE A HAND PROTECTOR FOR INSTALLATION OVER BAR STOCK. A WOODEN HAND PROTECTOR IS SUGGESTED, HOWEVER, ANY OTHER SUBSTITUTE MATERIAL MAY BE USED, SUCH AS A FLATTENED PIECE OF 0.0625 INCH BRASS SHEET STOCK WELDED TO BAR

32105

Figure 6-22. – Printed Circuit Board Puller

(g) The local oscillator A7 may be removed, after removing three mounting screws, by grasping top edge with fingers and pulling up.

(h) The local oscillator assembly A7 may be disassembled by removing the 10 screws holding the assembly together and then removing the printed circuit board A7A1. When reassembling the local oscillator assembly place the outer-most bottom edges on two flat surfaces prior to tightening the 10 screws to ensure proper seating when the local oscillator assembly is installed in the chassis. After insertion in the receiver replace the three mounting screws.

(i) Replace board by inserting in correct receptacle and pushing down with fingers until properly seated.

(j) Replace RFI cover on RF section and replace all mounting screws.

CAUTION. - Heed the CAUTION label located on right side of the receiver. The band change switches on all printed circuit boards in the RF section must be aligned correctly along with the slot in the band change gear box MP1 prior to inserting the band change shaft. Then carefully insert the shaft to prevent damage to the printed circuit boards.

Note: - When installing the band change shaft, the circuit boards in the RF section may need to be moved up and down to facilitate insertion.

(2) AF/IF Section Boards. - (See figure 6-4.) Remove the AF/IF section boards as follows:

(a) Remove mounting screws and top dust cover from receiver.

(b) Remove mounting screws and remove RFI cover from AF/IF section.

(c) Pull the board to be removed from chassis using appropriate board puller.

(d) Replace the board by inserting into correct receptacle and by pushing down with fingers until properly seated.

(e) Replace RFI cover on AF/IF section and replace all mounting screws.

(f) Replace top dust cover and mounting screws.

(3) Counter Section Boards. - (See figure 6-3.) Remove the counter section boards as follows:

(a) Remove mounting screws and top cover from receiver.

(b) Remove mounting screws and remove RFI cover from counter section.

(c) Pull board to be removed from chassis using appropriate board puller. Refer to paragraph 6-8f for instructions on removal of the entire counter A9.

(d) Replace board by inserting into correct receptacle and by pushing down with fingers until properly seated.

(e) Replace RFI cover on counter section and replace all mounting screws.

b. Front Panel. - The front panel must be partially removed for access to some replaceable subassemblies and components.

(1) Remove top dust cover and bottom dust/RFI cover from receiver.

(2) Remove the following front panel knobs:

(a) Loosen two screws and remove BAND-MHZ switch knob. Remove nut and washer securing switch shaft to front panel.

(b) Loosen two screws and remove the ANTENNA TRIM control, BFO KHZ control, LOCK-UNLOCK control, and the inner and outer TUNE control knobs from the front panel.

(3) Remove six mounting screws securing front panel to main chassis.

(4) Carefully pull front panel from the main chassis to the full extent of wire slack allowance.

(5) Replace front panel by reversing the procedures in steps (1) through (4).

c. BFO KHZ Capacitor C2. - (See figure 6-2.) Remove and replace BFO KHZ capacitor C2 as follows.

(1) Remove front panel as indicated in paragraph 6-8b.

(2) Remove BFO section RFI cover.

(3) Unsolder the two wires leading to the capacitor and label for replacement.

(4) Remove mounting screws and remove BFO KHZ capacitor from chassis.

(5) Replace BFO KHZ capacitor by reversing procedures of steps (1) through (3). Refer to wire list in Appendix B for wire destination if the wire labels are missing.

d. ANTENNA TRIM Capacitor C1. - (See figure 6-2.) Remove and replace ANTENNA TRIM capacitor C1 as follows:

(1) Remove front panel as indicated in paragraph 6-8b.

(2) Unsolder one wire and label for replacement.

(3) Remove ANTENNA TRIM capacitor C1 from chassis.

(4) Replace capacitor by reversing procedures of steps (1) and (3). Refer to wire list in Appendix B for wire destination if the wire label is missing.

e. Tuner Subassembly A21. - (See figure 6-16.) Remove and replace tuner subassembly as follows:

(1) Remove front panel as detailed in paragraph 6-8b.

(2) Remove dust cover from bottom of receiver.

(3) Remove BFO KHZ capacitor C2 as detailed in paragraph 6-8b.

(4) Remove ANTENNA TRIM capacitor C1 as detailed in paragraph 6-8c.

(5) Unsolder and label ten wires connected to connector assembly A16.

(6) Remove six mounting screws and remove the tuner subassembly A21 from chassis.

(7) Replace tuner subassembly in reverse order of steps (1) through (6). Refer to wire list in Appendix B for wire destinations if the wire labels are missing.

f. Counter A9. - (See figure 6-3.) Remove and replace counter A9 as follows:

WARNING

HIGH VOLTAGE (SPECIFICALLY +230 VDC) IS PRESENT IN COUNTER A9. DISCONNECT POWER WHEN REMOVING AND REPLACING COUNTER. CONTACT WITH THIS VOLTAGE COULD RESULT IN INJURY TO PERSONNEL.

(1) Remove top dust cover and bottom dust/RFI cover.

(2) Remove RFI cover from countersection.

(3) Remove two screws and disconnect plug A9P1 from J9 at bottom of receiver.

(4) Disconnect P1 from A9J1 at bottom of receiver.

(5) Remove gate generator board A9A2 and divider board A9A3 from counter using appropriate board puller.

(6) Remove six mounting screws at bottom of receiver securing counter to chassis.

(7) Remove two mounting screws from counter section.

(8) Remove counter A9 from chassis.

(9) The display board A9A1 may be now removed by removing seven mounting screws holding the display board to bracket. Unsolder and label all wires leading to components on the bracket.

(10) Remove RF oscillator by moving mounting screws, and unsoldering and labeling the two wires.

(11) Replace counter A9 and subassemblies in the reverse order of removal. Refer to wire list in Appendix B for wire destinations if the wire labels are missing.

g. Gear Assembly MP1. - (See figure 6-2.) Remove and replace the gear assembly MP1 as follows:

(1) Remove the top dust cover from receiver.

(2) Remove RFI cover from RF section.

(3) Set BAND-MHZ switch to 1.5-2.7.

(4) Remove shaft retainer and remove band change shaft from receiver.

(5) Loosen two screws holding band switch control shaft to gear assembly.

(6) Remove four screws holding gear assembly to chassis.

(7) When replacing the gear assembly, ensure that the slot for the tuning rod is rotated to the most vertical position. Replace gear assembly in the reverse order of steps (1) through (6).

h. Electrical RF Section Counter Assembly A16. - (See figure 6-16.) Remove and replace the electrical RF section connector assembly A16 located on the bottom of the receiver as follows:

(1) Remove mounting screws from rear end from the bottom of the receiver holding the bottom dust/RFI cover from receiver. Remove shield covering L.O. leads.

(2) Unsolder and label all wires leading from the connector assembly.

(3) Remove 16 mounting screws and remove connector assembly from receiver.

(4) Replace connector assembly in reverse order of removal. Refer to the wire list in appendix B for assistance in identifying the wires to be reconnected to the connector assembly.

i. Beat Frequency Oscillator (BFO) A22. (See figure 6-2.) Remove and replace BFO A22 as follows:

(1) Remove the top dust cover.

(2) Pull BFO board partially from chassis.

(3) Unsolder and label wires leading to the BFO board.

(4) Replace BFO printed circuit board in reverse order of removal. Refer to the wire list in Appendix B for assistance in identifying the wires to be reconnected to the BFO board A22.

j. Second Local Oscillator A18. - (See figure 6-4.) Remove and replace second local oscillator A18 from the receiver as follows:

(1) Remove the top and bottom dust covers from the receiver.

(2) Remove RFI cover from AF/IF section.

(3) Remove the four mounting screws and washers securing the second local oscillator to the chassis.

(4) Remove the local oscillator from chassis by grasping the top edge with fingers and pulling from chassis.

(5) Replace second local oscillator in chassis in the reverse order of removal.

k. Filters FL1 through FL3. - (See figure 1-2.) Remove and replace filters FL1 through FL3 as follows:

(1) Remove mounting screws and remove top dust cover and bottom dust/RFI cover from receiver.

(2) Remove RFI cover from RF section.

(3) Unsolder and label wires leading to filter to be removed at top and bottom of receiver.

(4) Remove nuts and washers holding filters to the filter retainer. This also releases shields of wires removed in step (3).

(5) At bottom of receiver, remove nuts and washers securing the filters to chassis.

(6) Remove the filter from chassis by grasping the top edge with fingers and pulling from chassis.

CAUTION. - When replacing filters FL1 through FL3, ensure that the OUTPUT end of the filter is at the top when inserted into receiver.

(7) Replace filter in chassis in the reverse order of removal. Refer to wire list in Appendix B for wire destinations if the wire labels are missing.

l. Filters FL4 through FL10. - (See figure 1-2.) Remove and replace filters FL4 through FL10 as follows:

(1) Remove mounting screws and remove top dust cover and bottom dust/RFI cover from receiver.

(2) Remove RFI cover from AF/IF section.

(3) Remove screws securing the filter retainer to chassis.

(4) Remove nuts and washers holding the filters to the filter retainer and remove filter retainer.

(5) At bottom of receiver, remove nuts and washers securing the filters to chassis.

(6) Remove the filter from chassis by grasping the top edge with fingers and pulling from chassis.

(7) Replace filter in chassis in the reverse order of removal.

m. Filter FL19. - (See figure 6-16.) Remove and replace filter FL19 as follows:

(1) Remove connector J2 from rear panel and unsolder and label wire leading to assembly A16. Remove connector J2 from cable.

(2) Remove nuts and washers holding filter to bottom of receiver.

(3) Remove filter with wires from receiver.

(4) Replace in reverse order of disassembly. Refer to wire list in appendix B for identification of connection point for wire going to assembly A16.

n. Lamp A21DS1. - (See figure 6-2.) Remove and replace lamp A21DS1 as follows:

(1) Remove two screws holding motion detector A21A1 on tuner subassembly A21.

(2) Pull motion detector A21A1 up from tuner subassembly A21 and turn to one side.

(3) Remove lamp A21DS1 from receptacle.

(4) Replace in reverse order of disassembly.

o. Power Supply PS1 or PS2. - (See figure 6-1.) Remove, disassemble, assemble, and replace power supplies PS1 and PS2 as follows:

(1) Remove mounting screws and remove top dust cover and remove bottom dust/RFI cover from receiver.

(2) Remove two mounting screws from bottom and four mounting screws from rear of receiver.

(3) Remove four screws that secure connectors P2 and P3 to J2 and J3, respectively, and disconnect P2 and P3 from power supply.

(4) Push up from bottom surface of power supply with fingers and remove power supply from receiver.

(5) Remove eleven screws holding cover to power supply and remove cover.

(6) Removal of Regulator Board A1. - (See figure 6-5)

(a) Remove three mounting screws holding board A1 to power supply chassis.

(b) Remove three stand-off nuts from board A1.

(c) Pull board A1 from power supply chassis and tilt to one side. This exposes wiring for unsoldering.

(d) Unsolder and label wires from board A1.

(e) Remove board A1 from power supply chassis.

(7) Removal of Regulator Board A2. - (See figure 6-5.)

(a) Remove regulator board A1 as detailed in paragraph 4-8p(5).

(b) Remove four mounting screws holding board A2 to power supply chassis.

(c) Pull board A2 slightly from power supply chassis and tilt to one side. This exposes wiring for unsoldering.

(d) Unsolder and label wires from board A2.

(8) Removal of Regulator Board A3 (PS2 only). - (See figure 6-5.)

(a) Remove regulator board A1 and A2 as detailed in paragraph 4-8p(5) and (6).

(b) Remove two mounting screws holding board A3 to power supply chassis.

(c) Pull board A3 slightly from chassis and tilt to one side. This exposes wiring for unsoldering.

(d) Unsolder and label wires from board A3.

(e) Remove board A3 from power supply chassis.

(9) Removal of transformer T1. - (See figure 6-5.)

(a) Remove regulator boards A1 and A2 from chassis as detailed in paragraphs 4-8p(5) and (6).

(b) Remove four mounting screws holding transformer T1 to chassis.

(c) Tilt transformer T1 to one side exposing wires for unsoldering.

(d) Unsolder and label wires from transformer T1.

(e) Remove transformer T1 from chassis.

(10) Reassemble and replace components of power supplies PS1 and PS2 in reverse order of removal and disassembly as detailed in steps (1) through (9). Refer to wire lists in Appendix B for wire destinations if the wire labels are missing.

6-9. GENERAL PARTS REPLACEMENT TECHNIQUES. - Most of the parts in the receiver can be reached easily and replaced without special purpose tools. The following precautions apply specifically to this receiver.

a. Before a part is removed, carefully note the position of the part and its leads. Install new parts in the same position as the original part to avoid unnecessary troubleshooting and rework.

b. When the feedthrough capacitors are being soldered, be careful to prevent the glass portion of the capacitor from cracking when the center conductor gets hot. Grasp the center lead with a pair of pliers between the glass bead and the wire to be attached before applying heat.

CAUTION. - Use a pencil-type soldering iron with a 25-watt maximum capacity. If only ac-operated soldering irons are available, use an isolating transformer. Do not use a soldering gun; damaging voltages can be induced in components.

c. When soldering transistor leads, solder quickly; where wiring permits, use a heat sink (such as long-noise pliers) between the soldered joint and the transistor. Use approximately the same length and dress of transistor leads as used originally.

6-10. PRINTED CIRCUIT CARD MAINTENANCE. - The following paragraphs contain instructions for printed circuit (PC) card maintenance, including component replacement and printed wiring repair.

a. Test Equipment and Special Tools Required. - Table 6-22 contains a list of equipment recommended for repair of PC cards.

Table 6-22. – Tools and Materials Required for Printed Circuit Card Repair.

NAME	MANUFACTURER'S DESIGNATION	USE
Pencil Soldering Iron 27-1/2 Watt	Ungar Model 776	Used for applying heat to solder joints
Chisel-Point Solder Tip, 1/4-inch Diameter	Ungar Model 1233	Used for applying solder to connection.
Thread-In Element For Desoldering Tipletts	Ungar Model 4045	Inserted in soldering pencil to hold and heat desoldering tipletts.
Thread-In Cone Tiplett, 3/8-inch Diameter	Ungar Model PL331	Applies heat to confined area, such as eyelets on circuit card.

Table 6-22. – Tools and Materials Required for Printed Circuit Card Repair. - Continued.

NAME	MANUFACTURER'S DESIGNATION	USE
Thread-In Cup Tiplett, 3/4-Inch Diameter	Ungar Model 855	Simultaneously applies heat to more than one contact when desoldering, such as for transistor connectors.
Thread-In Triangle Tiplett, 5/8-inch Diameter	Ungar Model 861	Simultaneously applies heat to more than one contact when desoldering.
Thread-In Bar Tiplett, 1-1/4 inch by 3/8 inch	Ungar Model 858	Simultaneously applies heat to more than one contact when desoldering. Used for removing relays.
Seizer (hemostatic), End-Straight-Nosed	Xcelite Model 43H	Used as a heat sink.
End-Cutting Diagonal Pliers, 4-1/2 inch	Klein Model 224	Used for clipping component leads on circuit cards.
Solder, Rosin Core	Kester Printed Circuit Solder No. 44	Used for soldering joints on circuit card.
Standard 6-inch Needle-Nose Pliers		General repair work.
Standard 6-inch Diagonal Electrician's Knife		General repair work.
Probe and Alignment Tool	General Cement GC9093	Used as soldering aid and probe.
Scraper and Brush Tool	General Cement GC9094	Used as soldering aid, circuit card scraper, and cleaner.
Flux Remover		
Solder-Wick	Solder Removal Co. Catalog No. 40-3-5	Used for removing solder
Silicon Adhesive-Sealant, Translucent	MIL-A-46106 Translucent	Coats repaired area on board.

b. Printed Circuit Card Part Removal. - To remove a part from a PC card, proceed as follows:

(1) With end-cutting diagonal pliers, clip leads of part to be replaced. Leave sufficient lead so that it can be gripped with long-noise pliers.

(2) Remove circuit part. If bonded to circuit card, insert blade of pocket knife between card and part and lightly pry up. If part does not free easily, apply pencil soldering iron and move it along bond to soften bonding substance.

CAUTION. - To prevent damage to card, do not hold soldering iron in one place longer than 8 seconds.

(3) Use appropriate desoldering tiplett, apply heat to soldered joints, and remove clipped leads.

CAUTION. - To prevent damage to eyelet, do not hold soldering iron on eyelet longer than 6 seconds.

(4) Remove leads soldered to eyelets from bottom of card.

(5) Gently clean eyelets with scraper and/or probe and alignment tool, brush tool, and soldering iron. The card is now ready for replacement part.

c. Printed Circuit Card Part Replacement. - To replace a circuit part, proceed as follows:

(1) Measure distance between eyelets that are to receive part.

(2) Cut excess lead from part. Allow about 1/4-inch feedthrough of leads in eyelets.

(3) Insert part. If part has directional characteristics, check to be sure part is inserted correctly.

(4) After part is inserted, seat it firmly and bend leads slightly away from part.

(5) Place solder on eyelet and using chisel-point solder tip, place iron on solder. If part is heat sensitive, clamp seizer between part and solder joint. Hold soldering iron on joint for 3 to 5 seconds. A proper solder connection displays an even flow around joint and appears glossy when cool.

(6) Clip excess lead from soldered joint.

(7) Clean board with flux remover.

(8) Coat repaired area with silicon sealant to seal bond.

d. Printed Wiring Repair. - Table 6-23 lists the tools and materials recommended for printed wiring repair. To repair broken printed wiring, proceed as follows:

(1) With pocket-knife blade, lightly scrape insulating material on printed wire. Remove insulating material along wire 1/4-inch on both sides of break.

(2) If break is no more than a slight crack, place solder on break and apply soldering iron.

Table 6-23. – Tools and Materials Required for Printed Wiring Repair.

NAME	MANUFACTURER'S DESIGNATION	USE
Electrician's Pocket Knife	GFE	General repair
Solder, Rosin Core	Kester Printed Circuit Solder No. 44	Joins broken printed wiring.
Insulating Varnish	GFE (MIL-V-1137A)	Insulates bare wiring.
Pencil Soldering Iron	Ungar Model 776	Used for soldering printed wiring.
Chisel-Point Solder Tip, 1/4-inch Diameter	Ungar Model 1233	Used for pencil soldering iron.
Printed Circuit Board Fixture	Technical Devices	Holds circuit card.

CAUTION. - To prevent damage to printed wire, do not hold soldering iron on longer than 3 to 5 seconds.

(3) If break is too large to be repaired by drop of solder, place 1/2-inch piece of stripped No. 24 AWG wire across break on printed wire. Apply solder to ends of wire and printed wire and hold soldering iron on solder for 3 to 5 seconds.

(4) When soldering joints have cooled, clean with flux remover.

(5) Coat repaired area with silicone sealant to seal board.